phyCARD®-i.MX 6

Hardware Manual

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Preliminary

Preliminary Edition August 2014

List of Figures ..... **iii**
List of Tables ..... **iv**
Conventions, Abbreviations and Acronyms ..... **vii**
Preface ..... **ix**
1 Introduction **1**
1.1 Block Diagram 3
1.2 View of the phyCARD-i.MX 6 4
1.3 Minimum Requirements to Operate the phyCARD-i.MX 6 6
2 Pin Description **7**
3 Jumpers **13**
4 Power **17**
4.1 Primary System Power (VDD_3V3) 17
4.2 Backup Voltage (VSTBY) 18
4.3 Power Management IC (U29) / Control Management IC (U17) 18
4.3.1 Power Management IC (PMIC, U29) 18
4.3.2 Control Management IC (CMIC, U17) 18
4.3.3 Power Domains 19
4.4 Supply Voltage for external Logic 21
5 Power Management **23**
6 System Configuration and Booting **25**
7 System Memory **27**
7.1 DDR3 SDRAM (U2-U9) 27
7.2 NAND Flash Memory (U13) 27
7.3 I²C EEPROM (U10) 28
7.3.1 EEPROM Write Protection Control (J3) 28
8 SD / MMC Card Interfaces **29**
9 Serial Interfaces **31**
9.1 Universal Asynchronous Interface 32
9.2 USB OTG Interface 32
9.3 USB Host Interface 33
9.4 Ethernet Interface 34
9.4.1 Ethernet PHY (U11) 34
9.4.2 MAC Address 35
9.5 I^2C Interface 35
9.6 SPI Interface 36
9.7 I^2S Audio Interface (SSI) 36
10 General Purpose I/Os **38**
11 User LEDs **39**
12 Debug Interface (X3)) **40**
13 LVDS Display Interface **43**
13.1 LVDS Display Interface pixel mapping 43
14 LVDS Camera Interface **45**
14.1 Signal Configuration (J31) 45
15 Technical Specifications **46**

Preliminary

16 Hints for Integrating and Handling the phyCARD-i.MX 6 50
16.1 Integrating the phyCARD-i.MX 6 50
16.2 Handling the phyCARD-i.MX 6 52
17 The phyCARD-i.MX 6 on the phyBASE 54
17.1 Concept of the phyBASE Board 55
17.2 Overview of the phyBASE Peripherals 56
17.2.1 Connectors and Pin Header 57
17.2.2 Switches 58
17.2.3 LEDs 60
17.2.4 Jumpers 61
17.3 Functional Components on the phyBASE Board 65
17.3.1 phyCARD-i.MX 6 SOM Connectivity (X27) 65
17.3.2 Power Supply (X28) 66
17.3.3 RS-232 Connectivity (P1) 68
17.3.4 Ethernet Connectivity (X10) 69
17.3.5 USB Host Connectivity (X6, X7, X8, X9, X33) 70
17.3.6 USB OTG Connectivity (X29) 72
17.3.7 Display / Touch Connectivity (X6, X32) 73
17.3.7.1 PDI Data Connector (X6) 74
17.3.7.2 Display Power Connector (X32) 76
17.3.7.3 Touch Screen Connectivity 77
17.3.8 Audio Interface (X1, X2, X3) 78
17.3.9 I^2C Connectivity 80
17.3.10 SPI Connectivity 82
17.3.11 User programmable GPIOs 82
17.3.12 Extension connectors (X8A, X9A) 83
17.3.13 Secure Digital Memory Card/ MultiMedia Card (X26) 85
17.3.14 Boot Mode Selection (JP1) 86
17.3.15 System Reset Button (S1) 88
17.3.16 RTC at U3 89
17.3.17 PLD at U25 91
17.3.18 Carrier Board Physical Dimensions 92
18 Revision History 93
Index 95

Preliminary

List of Figures

Figure 1: Block Diagram of the phyCARD-i.MX 6 3
Figure 2: phyCARD-i.MX 6 Component Placement (top view) 4
Figure 3: phyCARD-i.MX 6 Component Placement (bottom view) 5
Figure 4: Pinout of the phyCARD-Connector (top view, with cross section insert) 8
Figure 5: Typical Jumper Pad Numbering Scheme 13
Figure 6: Jumper Locations (top view) 14
Figure 7: Jumper Locations (bottom view) 15
Figure 8: Power Supply Diagram 20
Figure 9: JTAG Interface at X2 and X3 (top view) 40
Figure 10: JTAG Interface at X2 and X3 (bottom view) 41
Figure 11: Physical Dimensions 46
Figure 12: Footprint of the phyCARD-i.MX 6 51
Figure 13: phyBASE Overview of Connectors, LEDs and Buttons 56
Figure 14: Typical Jumper Numbering Scheme 61
Figure 15: phyBASE Jumper Locations 62
Figure 16: phyCARD-i.MX 6 SOM Connectivity to the Carrier Board 65
Figure 17: Powering Scheme 66
Figure 18: Power Connector corresponding to Wall Adapter Input X28 66
Figure 19: RS-232 Interface Connector P1 68
Figure 20: RS-232 Connector P1 Signal Mapping 68
Figure 21: Ethernet Interface at Connector X10 69
Figure 22: Components supporting the USB Host Interface 70
Figure 23: USB OTG Interface at Connector X29 72
Figure 24: Universal LVDS Interface at Connector X6 73
Figure 25: Audio Interface at Connectors X1, X2, X3 78
Figure 26: Extension Connector X8A, X9A 83
Figure 27: SD / MM Card interface at connector X26 85
Figure 28: Boot Mode Selection Jumper JP1 86
Figure 29: System Reset Button S1 88
Figure 30: RTC with Battery Buffer 89
Figure 31: Carrier Board Physical Dimensions 92

Preliminary

List of Tables

Table 1: Abbreviations and Acronyms used in this Manual viii
Table 2: X-Arc Bus Pinout 9
Table 3: Pinout of the phyCARD-Connector X1, Row A 10
Table 4: Pinout of the phyCARD-Connector X1, Row B 11
Table 5: Jumper Settings 16
Table 6: Power Management Pins 23
Table 7: Power States 23
Table 8: Boot Modes of the phyCARD-i.MX 6 26
Table 9: Boot Configuration Signals generated by the CM 26
Table 10: EEPROM write protection states via J3 28
Table 11: Location of SD/ MMC Card Interface Signals 29
Table 12: Location of the UART Signals 32
Table 13: Location of the USB OTG Signals 33
Table 14: Location of the USB-Host Signals 33
Table 15: Location of the Ethernet Signals 34
Table 16: I^2C Interface Signal Location 35
Table 17: SPI Interface Signal Location 36
Table 18: SSI Interface Signal Location 37
Table 19: Location of GPIO and IRQ pins 38
Table 20: JTAG Connector X3 Signal Assignment 42
Table 21: Debug interface Connector X2 Signal Assignment 42
Table 22: Display Interface Signal Location 43
Table 23: Pixel Mapping of 18-bit LVDS Display Interface 44
Table 24: Pixel Mapping of 24-bit LVDS Display Interface 44
Table 25: Camera Interface Signal Location at X1 45
Table 26: LVDS Signal Configuration J31 45
Table 27: phyBASE Connectors and Pin Headers 57
Table 28: phyBASE Push Buttons Descriptions 58
Table 29: phyBASE DIP-Switch S3 Descriptions 59
Table 30: phyBASE LEDs Descriptions 60
Table 31: phyBASE Jumper Descriptions 63
Table 32: LEDs Assembled on the Carrier Board 67
Table 33: Distribution of the USB Hub's (U4) Ports 71

Preliminary

Table 34: Universal USB Pin Header X33 Signal Description 71
Table 35: Display Data Connector X6 Signal Description 74
Table 36: Auxiliary Interfaces at PDI Data Connector X12 75
Table 37: SPI and GPIO Connector Selection 76
Table 38: LVDS Power Connector X32 Signal Description....76
Table 39: Selection of the Touch Screen Controller....77
Table 40: Selection of the Audio Codec 79
Table 41: I^2C Connectivity 80
Table 42: I^2C Addresses in Use 80
Table 43: SPI Connector Selection 82
Table 44: SPI and GPIO Connector Selection 84
Table 45: PHYTEC Extension Connectors X8A, X9A 84
Table 46: Boot Options for the phyCARD-i.MX 6 87

Preliminary

Preliminary

Conventions, Abbreviations and Acronyms

This hardware manual describes the PCA-A-XS1 System on Module in the following referred to as phyCARD®-i.MX 6. The manual specifies the phyCARD®-i.MX 6's design and function. Precise specifications for the Freescale Semiconductor i.MX 6 microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{\text{RD}}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device.
- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyCARD-Connector always refer to the high density molex connector on the undersides of the phyCARD-i.MX 6 System on Module.

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Preliminary

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows, or Linux) preinstalled on the module and Development Tools).
CB	Carrier Board; used in reference to the phyBASE Development Kit Carrier Board.
DFF	D flip-flop.
EMB	External memory bus.
EMI	Electromagnetic Interference.
GPI	General purpose input.
GPIO	General purpose input and output.
GPO	General purpose output.
IRAM	Internal RAM; the internal static RAM on the Freescale Semiconductor i.MX 6 microcontroller.
J	Solder jumper; these types of jumpers require solder equipment to remove and place.
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools.
PCB	Printed circuit board.
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards, or custom adapters
PEB	PHYTEC Extension Board
PMIC	Power management IC
PoE	Power over Ethernet
PoP	Package on Package
POR	Power-on reset
RTC	Real-time clock.
SMT	Surface mount technology.
SOM	System on Module; used in reference to the PCA-A-XS1 /phyCARD®-i.MX 6 module
Sx	User button Sx (e.g. S1, S2) used in reference to the available user buttons, or DIP-Switches on the CB.
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board.
VSTBY	SOM standby voltage input

Table 1: Abbreviations and Acronyms used in this Manual

Note: The BSP delivered with the phyCARD®-i.MX 6 usually includes drivers and/or software for controlling all components such as interfaces, memory, etc. Therefore programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the i.MX 6 Reference Manual, if such information is needed to connect customer designed applications.

Preliminary

Preface

As a member of PHYTEC's new phyCARD® product family the phyCARD-i.MX 6 is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCARD® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyCARD® module lies in its layout and test.

PHYTEC's new phyCARD® product family consists of a series of extremely compact embedded control engines featuring various processing performance classes while using the newly developed X-Arc embedded bus standard. The standardized connector footprint and pin assignment of the X-Arc bus makes this new SOM generation extremely scalable and flexible. This also allows to use the same carrier board to create different applications depending on the required processing power. With this new SOM concept it is possible to design entire embedded product families around vastly different processor performances while optimizing overall system cost. In addition, future advances in processor technology are already considered with this new embedded bus standard making product upgrades very easy. Another major advantage is the forgone risk of potential system hardware redesign steps caused by processor or other critical component discontinuation. Just use one of PHYTEC's other phyCARD® SOMs thereby ensuring an extended product life cycle of your embedded application.
Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce your development time and risk and allow you to focus on your product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution you will be able to bring your new ideas to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html or
www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Preliminary

Ordering Information

The part numbering of the phyCARD has the following structure:

PCA-A-XL3-*xxxxxx*

Generation

A = First generation

Performance class

XS = lowest
S = low
M = middle
L = high
XL = highest

Controller No. of specified performance class and

Assembly options (depending on model)

In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at

http://www.phytec.de/de/support/registrierung.html or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our web site which provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/de/support/faq/faq-phyCARD-i.MX 6.html or
http://www.phytec.eu/europe/support/faq/faq-phyCARD-i.MX 6.html

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Declaration of Electro Magnetic Conformity of the PHYTEC phyCARD®-i.MX 6

PHYTEC System on Module (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Product Change Management and information in this manual on parts populated on the SOM

When buying a PHYTEC SOM, you will, in addition to our HW and SW offerings, receive a free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) Team of developers, is continuously processing, all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are being evaluated in order to take the right masseurs in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Preliminary

Therefore we have established a set of methods to fulfill our philosophy:

Avoiding strategies

- Avoid changes by evaluating long-livety of parts during design in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management in case of functional changes

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating changes through HW redesign or backward compatible SW maintenance.
- Provide early change notifications concerning functional relevant changes of our products.

Change management in rare event of an obsolete and non replaceable part

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Therefore we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

Preliminary

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1 Introduction

The phyCARD-i.MX 6 belongs to PHYTEC's phyCARD System on Module family. The phyCARD SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCARD boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

PHYTEC's phyCARD family introduces the newly developed X-Arc embedded bus standard. Apart from processor performance, a large number of embedded solutions require a corresponding number of standard interfaces. Among these process interfaces are for example Ethernet, USB, UART, SPI, I^2C, audio, display and camera connectivity. The X-Arc bus exactly meets this requirement. As well the location of the commonly used interfaces as the mechanical specifications are clearly defined. All interface signals of PHYTEC's new X-Arc bus are available on a single, 100-pin , high-density pitch (0.635 mm) connector, allowing the phyCARDs to be plugged like a "big chip" into a target application. The reduced complexity of the phyCARD SOM as well as the smaller number of interface signals greatly simplifies the SOM carrier board design helping you to reduce your time-to-market.

As independent research indicates that approximately 70% of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments approximately 20% of all pin header connectors on the X-Arc bus are dedicated to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCARD boards even in high noise environments.

phyCARD boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyCARD users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCARD-i.MX 6 is a subminiature (60 mm x 60 mm) insert-ready System on Module populated with the Freescale Semiconductor i.MX 6 microcontroller. Its universal design enables its insertion in a wide range of embedded applications.

Precise specifications for the controller populating the board can be found in the applicable controller Reference Manual or datasheet. The descriptions in this manual are based on the Freescale Semiconductor i.MX 6. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCARD-i.MX 6.

Preliminary

The phyCARD-i.MX 6 offers the following features:

- Subminiature System on Module (60 mm x 60 mm) achieved through modern SMD technology
- Populated with the Freescale Semiconductor i.MX 6 microcontroller (BGA624 packaging)
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- X-Arc bus including commonly used interfaces such as Ethernet, USB, UART, SPI, I^2C, audio, camera and display connectivity (LVDS) available at one 100-pin high-density (0.635 mm) Molex connector, enabling the phyCARD-i.MX 6 to be plugged like a "big chip" into the target application
- Max. 1 GHz core clock frequency
- Boot from different memory devices (NAND Flash (standard))
- RAM memory device with 512 MB (up to 4 GB) DDR3 SDRAM
- 256 MB (up to 4 GB) on-board NAND Flash (VFBGA)
- Up to 32 Kbit I^2C EEPROM
- Serial interface with 4 lines (TTL) allowing simple hardware handshake
- High-Speed USB OTG interface
- High-Speed USB HOST interface
- Auto HDX/FDX 10/100MBit Ethernet interface, with HP Auto MDI/MDI-X support
- One I^2C interfaces
- One SPI interfaces
- I^2S (SSI) audio interface
- 4 channel LVDS (24 bit) LCD interface
- LVDS camera interface; phyCAM-S(+) compatible
- SD/MMC card interface with DMA
- Support of standard 20 pin debug interface through JTAG connector
- Additional serial interface connector for debugging
- 3 GPIO/IRQ ports
- 2 Power State outputs to support applications requiring a power management
- 1 Wake Up input
- Two user programmable LEDs
- Single supply voltage of 3.3 V (max 1.5 A).
- All controller required supplies are generated on board
- On-board power management IC (PMIC) with integrated RTC
- Control Management IC (CMIC)
- Industrial temperature range (-40°C..+80°C)

Preliminary

1.1 Block Diagram

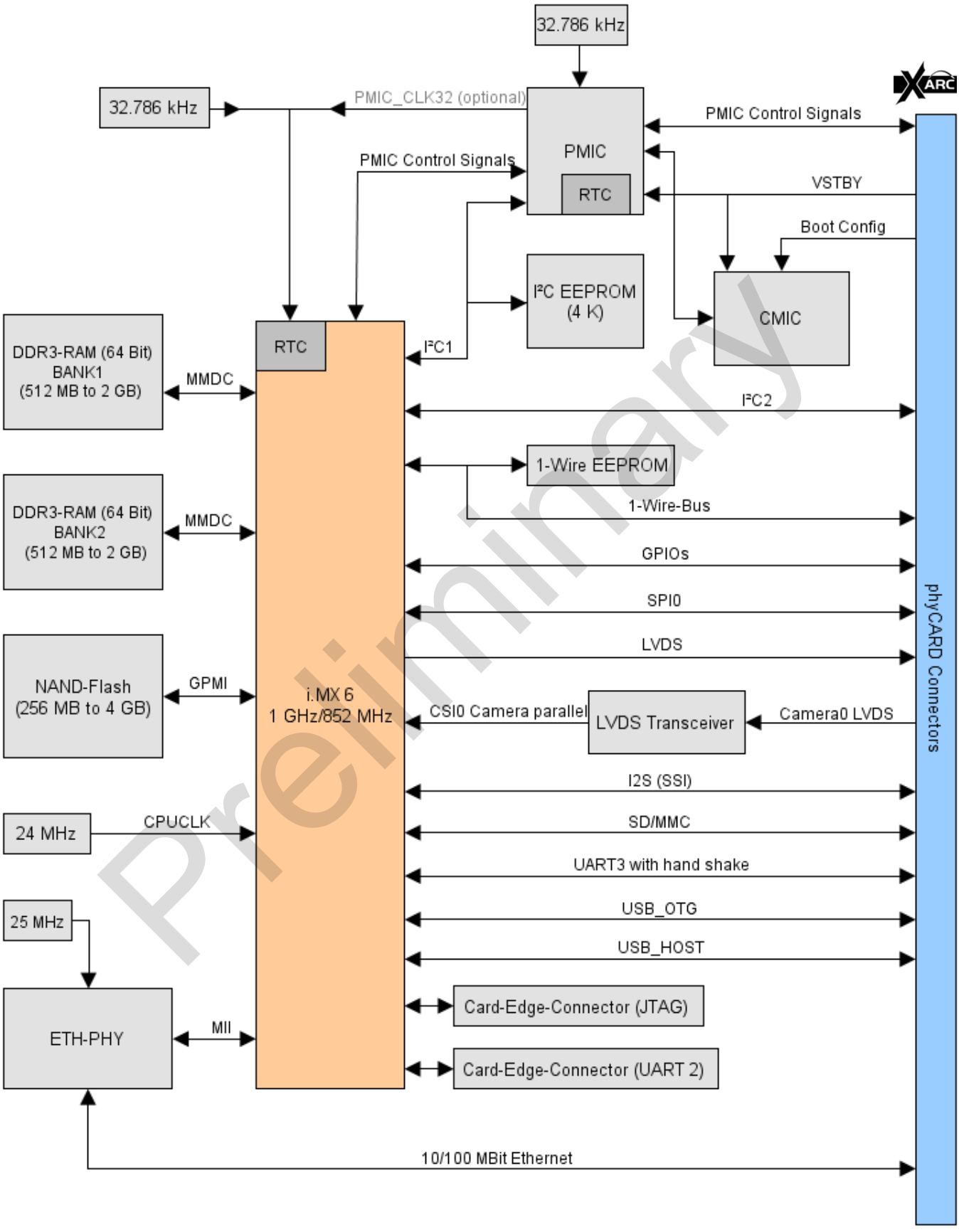

Figure 1: Block Diagram of the phyCARD-i.MX 6

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1.2 View of the phyCARD-i.MX 6

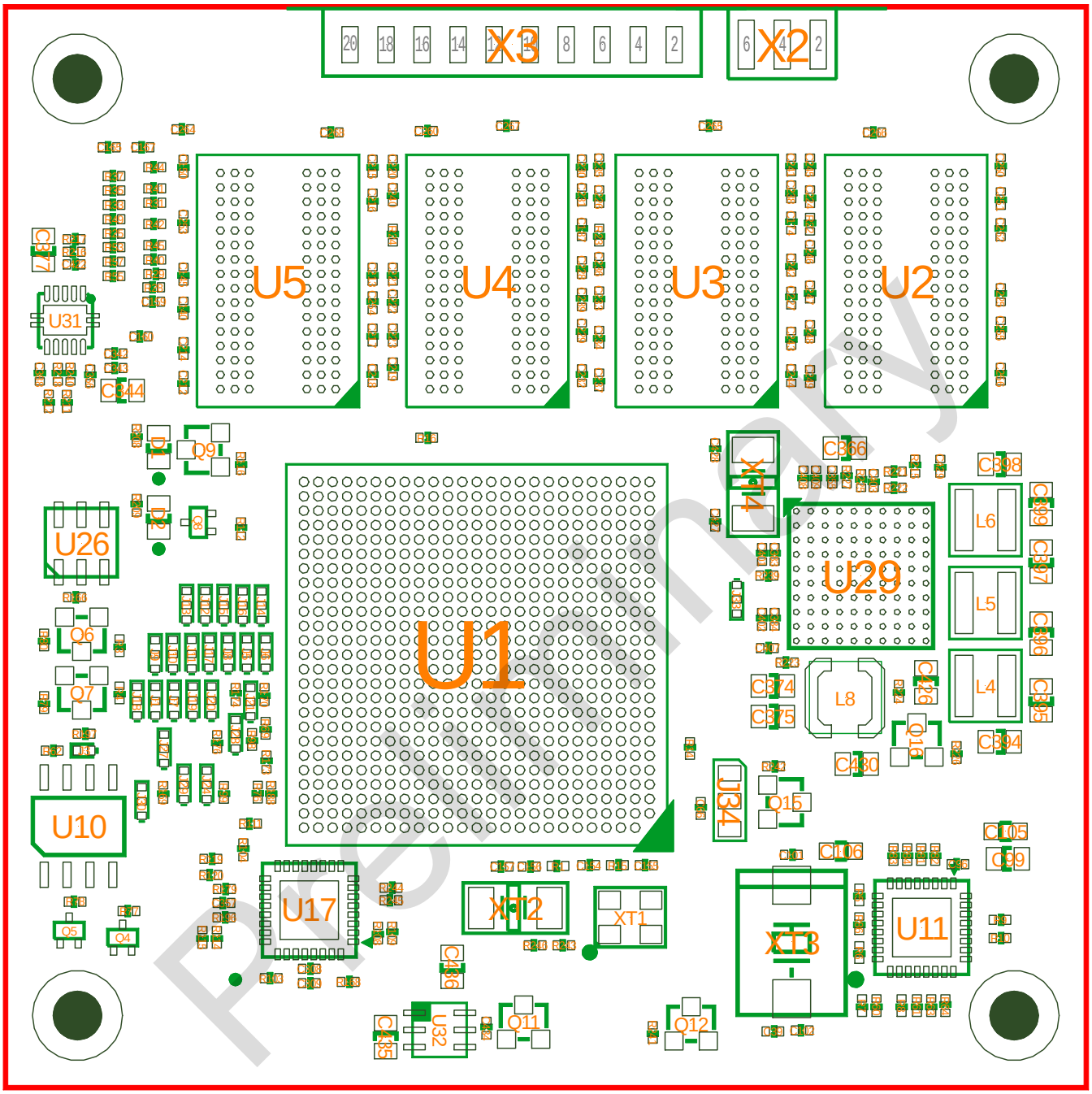

Figure 2: phyCARD-i.MX 6 Component Placement (top view)

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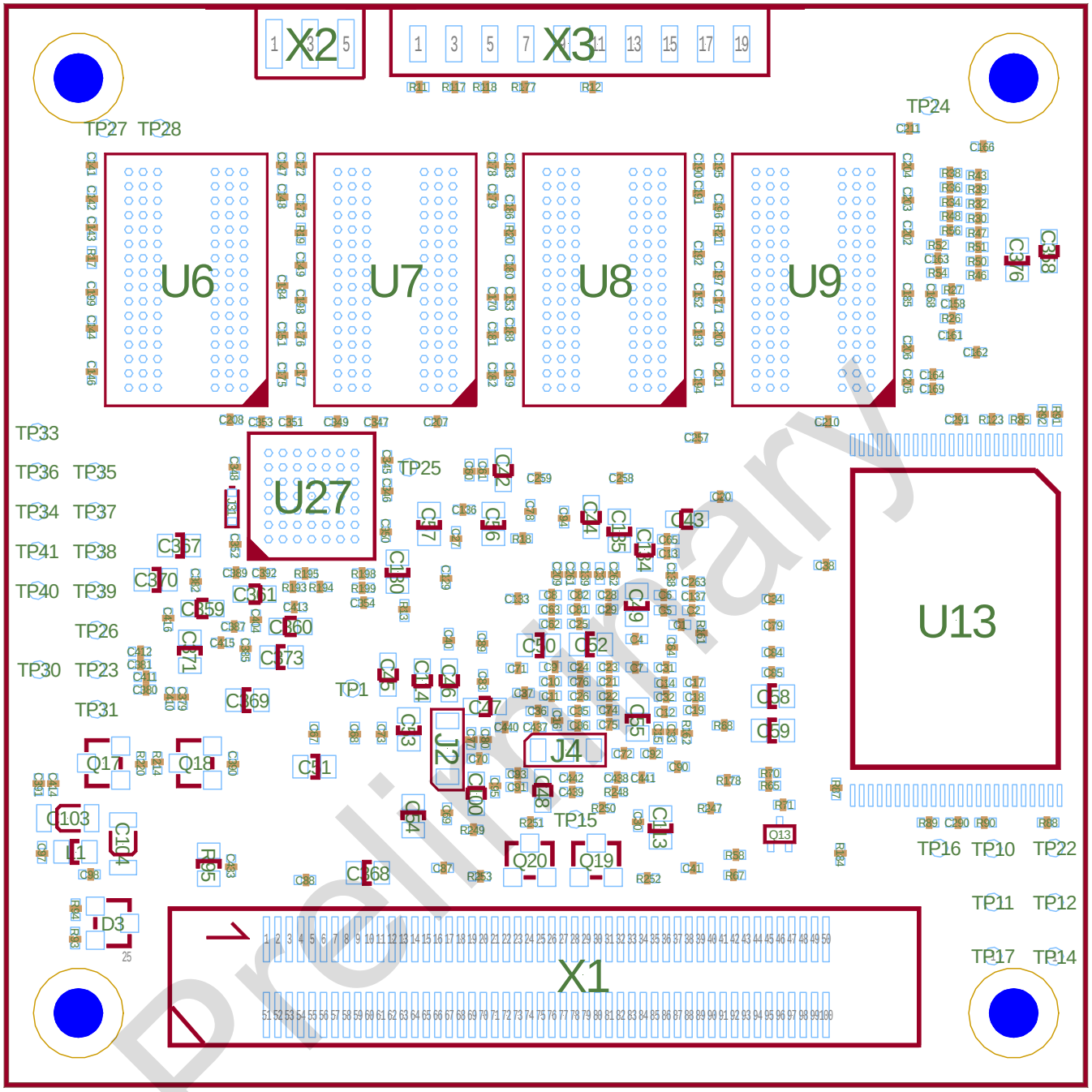

Figure 3: phyCARD-i.MX 6 Component Placement (bottom view)

1.3 Minimum Requirements to Operate the phyCARD-i.MX 6

Basic operation of the phyCARD-i.MX 6 only requires supply of a +3.3 V input voltage with 1.5 A load and the corresponding GND connection.

These supply pins are located at the phyCARD-Connector X1:

VDD_3V3: X1 1A, 2A, 3A, 1B, 2B, 3B

Connect all +3.3 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 4A, 8A, 13A, 4B, 8B, 13B

Please refer to *section 2* for information on additional GND Pins located at the phyCARD-Connector X1.

Caution:
We recommend connecting all available +3.3 V input pins to the power supply system on a custom carrier board housing the phyCARD-i.MX 6 and at least the matching number of GND pins neighboring the +3.3 V pins.

In addition, proper implementation of the phyCARD-i.MX 6 module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to *section 4* for more information.

Preliminary

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all X-Arc bus signals extend to one surface mount technology (SMT) connector (0.635 mm) lining on side of the module (referred to as phyCARD-Connector). This allows the phyCARD-i.MX 6 to be plugged into any target application like a "big chip".

The numbering scheme for the phyCARD-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (refer to *Figure 4*).

The numbered matrix can be aligned with the phyCARD-i.MX 6 (viewed from above; phyCARD-Connector pointing down) or with the socket of the corresponding phyCARD Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCARD-i.MX 6 marked with "1A". The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCARD-Connector as well as the mating connector on the phyCARD Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCARD-Connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCARD-Connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector.

The following figure illustrates the numbered matrix system. It shows a phyCARD-i.MX 6 with an SMT phyCARD-Connector on its underside (defined as dotted lines) mounted on a carrier board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCARD-i.MX 6 module showing the phyCARD-Connector mounted on the underside of the module's PCB.

Preliminary

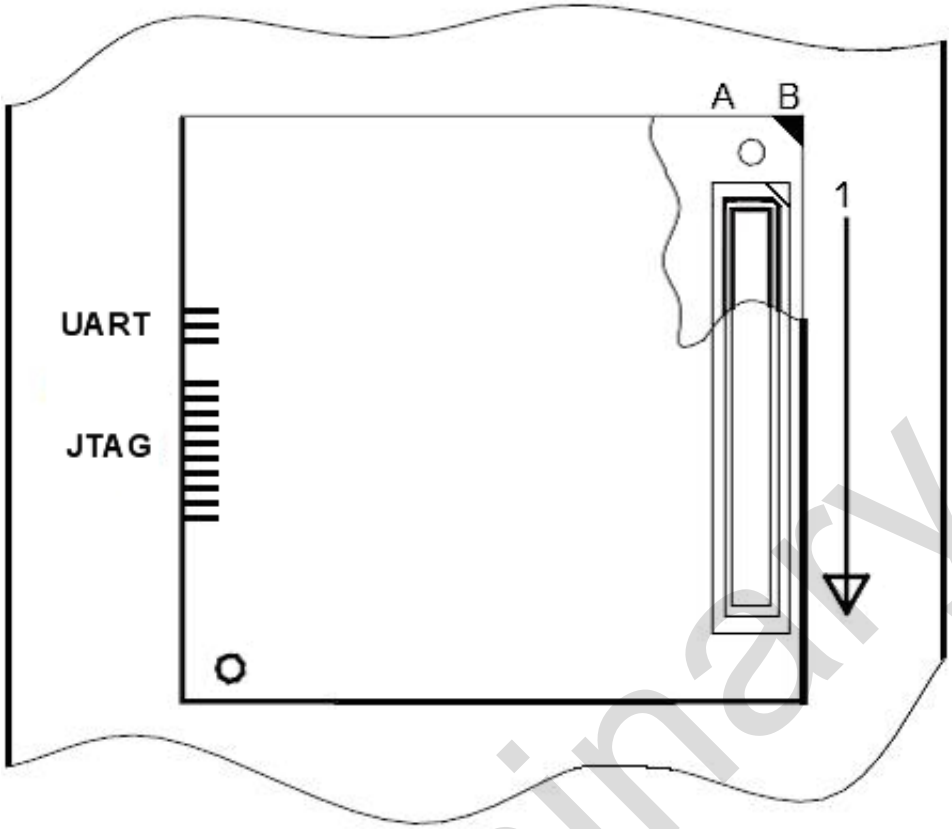

Figure 4: Pinout of the phyCARD-Connector (top view, with cross section insert)

Table 2 shows the pinout of the X-Arc bus with the functional grouping of the signals, while *Table 3* and *Table 4* provide an overview of the pinout of the phyCARD-Connector with signal names and descriptions specific to the phyCARD-i.MX 6. They also provide the appropriate signal level interface voltages listed in the SL (Signal Level) column and the signal direction.

The Freescale Semiconductor i.MX 6 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *Freescale Semiconductor i.MX 6 Reference Manual* for details on the functions and features of controller signals and port pins.

Preliminary

	I/O	Signal	Pin	Pin	Signal	I/O	
Supply	In	VCC	1A	1B	VCC	In	Supply
	In	VCC	2A	2B	VCC	In	
	In	VCC	3A	3B	VCC	In	
	-	GND	4A	4B	GND	-	
	Out	VCC_LOGIC	5A	5B	VCC_LOGIC	Out	
	-	FEEDBACK	6A	6B	VSTBY	In	
	In	nRESET_IN	7A	7B	nRESET_OUT	Out	
	-	GND	8A	8B	GND	-	
Display	Out	LVDS_TX0+	9A	9B	LVDS_TX1+	Out	Display
	Out	LVDS_TX0-	10A	10B	LVDS_TX1-	Out	
	Out	LVDS_TX2+	11A	11B	LVDS_TX3+	Out	
	Out	LVDS_TX2-	12A	12B	LVDS_TX3-	Out	
	-	GND	13A	13B	GND	-	
	Out	LVDS_TXCLK+	14A	14B	LVDS_CAM_RX+	In	Camera
	Out	LVDS_TXCLK-	15A	15B	LVDS_CAM_RX-	In	
Camera	Out	LVDS_CAM_MCLK	16A	16B	LVDS_CAM_nLOCK	Out	
I²C	Bi	I2C_CLK	17A	17B	I2C_DATA	Bi	I²C
	-	GND	18A	18B	GND	-	
Ethernet	Out	ETH_SPEED	19A	19B	ETH_LINK	Out	Ethernet
	Out	ETH_TX+	20A	20B	ETH_RX+	In	
	Out	ETH_TX-	21A	21B	ETH_RX-	In	
	-	GND	22A	22B	GND	-	
USB OTG	Out	nUSB_OTG_PWR	23A	23B	nUSB_HOST_PWR	Out	USB Host
	In	nUSB_OTG_OC	24A	24B	nUSB_HOST_OC	In	
	-	GND	25A	25B	GND	-	
	Bi	USB_OTG_VBUS	26A	26B	nSuspend_to_RAM	Out	
	Bi	USB_OTG_D-	27A	27B	USB_HOST_D-	Bi	USB Host
	Bi	USB_OTG_D+	28A	28B	USB_HOST_D+	Bi	
	In	USB_OTG_UID1	29A	29B	nPower_Off	Out	
	-	GND	30A	30B	GND	-	
SD/MMC	Bi	SDIO_D0	31A	31B	SDIO_D1	Bi	SD/MMC
	Bi	SDIO_D2	32A	32B	SDIO_D3	Bi	
	Out	SDIO_CLK	33A	33B	SDIO_CMD	Bi	
	-	GND	34A	34B	GND	-	
SPI	Out	SPI_CS0	35A	35B	SPI_CS1	Out	SPI
	In	SPI_RDY	36A	36B	SPI_MOSI	Out	
	Out	SPI_CLK	37A	37B	SPI_MISO	In	
	-	GND	38A	38B	GND	-	
UART	Out	UART_TXD	39A	39B	UART_RXD	In	UART
	In	UART_RTS	40A	40B	UART_CTS	Out	
	-	GND	41A	41B	GND	-	
AC'97/I²S	Bi	I2S_SEL/AC97_INT	42A	42B	AC97/I2S_BIT_CLK	Bi	AC'97/I²S
	Out	AC97/I2S_SDATA_OUT	43A	43B	AC97/I2S_SYNC	Out	
	In	AC97/I2S_SDATA_IN	44A	44B	AC97/I2S_nRESET	Out	
	-	GND	45A	45B	GND	-	
GPIO	Bi	GPIO0/IRQ	46A	46B	SDIO_CD	In	SD/MMC
	Bi	GPIO2/IRQ/PWM	47A	47B	GPIO1/IRQ	Bi	GPIO
	In	nWKUP	48A	48B	for internal use only	Bi	
	-	GND	49A	49B	GND	-	
Boot Opt.	In	CONFIG0	50A	50B	CONFIG1	In	Boot Opt.

Preliminary

Table 2: X-Arc Bus Pinout

Note:
SL is short for Signal Level (V) and is the applicable logic level to interface a given pin. Those pins marked as "N/A" have a range of applicable values that constitute proper operation.

Please refer to the phyCARD Design-In Guide (LAN-051) for layout recommendations and example circuitry.

Pin Row X1A				
Pin #	Signal	I/O	SL	Description
1A	VDD_3V3	I	Power	3.3 V Primary voltage supply input
2A	VDD_3V3	I	Power	3.3 V Primary voltage supply input
3A	VDD_3V3	I	Power	3.3 V Primary voltage supply input
4A	GND	-	-	Ground 0 V
5A	VDD_3V3_LOGIC[1]	O	Power	VCC Logic output
6A	FEEDBACK	O	Power	Feedback output to indicate the supply voltage required (floating in order to configure the CB or target application for 3.3 V)
7A	X_nRESET_IN	I	VBAT	Active low Reset In
8A	GND	-	Power	Ground 0 V
9A	X_LVDS_TX0+	O	LVDS	LVDS Chanel 0 positive output
10A	X_LVDS_TX0-	O	LVDS	LVDS Chanel 0 negative output
11A	X_LVDS_TX2+	O	LVDS	LVDS Chanel 2 positive output
12A	X_LVDS_TX2-	O	LVDS	LVDS Chanel 2 negative Output
13A	GND	-	Power	Ground 0V
14A	X_LVDS_TXCLK+	O	LVDS	LVDS Clock positive output
15A	X_LVDS_TXCLK-	O	LVDS	LVDS Clock negative output
16A	X_LVDS_CAM_MCLK		VDD_3V3_LOGIC	Camera master clock output
17A	X_I2C_CLK	O	VDD_3V3_LOGIC	I2C2 Clock output
18A	GND	-	Power	Ground 0 V
19A	X_ETH_SPEED	O	VDD_ETH_3V3	Ethernet speed indicator (open drain)
20A	X_ETH_TX+	O (I)	VDD_ETH_3V3	Transmit positive output (normal) Receive positive input (reversed)
21A	X_ETH_TX-	O (I)	VDD_ETH_3V3	Transmit negative output (normal) Receive negative input (reversed)
22A	GND	-	Power	Ground 0 V
23A	X_nUSB_OTG_PWR	O	VDD_3V3_LOGIC	USB-OTG power switch output open drain
24A	X_nUSB_OTG_OC	I	VDD_3V3_LOGIC	USB-OTG over current input signal
25A	GND	-	Power	Ground 0 V
26A	X_USB_OTG_VBUS	I	Power	USB OTG VBUS voltage (5 V optional)
27A	X_USB_OTG_D-	I/O	USB	USB OTG transceiver cable interface, D-
28A	X_USB_OTG_D+	I/O	USB	USB OTG transceiver cable interface, D+
29A	X_USB_OTG_UID	I	VDD_3V3_LOGIC	USB OTG on the go transceiver cable ID resistor connection
30A	GND	-	Power	Ground 0 V

Table 3: Pinout of the phyCARD-Connector X1, Row A

[1]: Caution! The current draw at VDD_3V3_LOGIC must not exceed 500 mA.

Preliminary

Pin Row X1A				
Pin #	Signal	I/O	SL	Description
31A	X_SDIO_D0	I/O	VDD_3V3_LOGIC	SD/MMC Data line D0 both in 1-bit and 4-bit mode
32A	X_SDIO_D2	I/O	VDD_3V3_LOGIC	SD/MMC Data line D 2both in 1-bit and 4-bit mode
33A	X_SDIO_CLK	O	VDD_3V3_LOGIC	SD/MMC Clock for MMC/SD/SDIO
34A	GND	-	Power	Ground 0 V
35A	X_SPI_CS0	O	VDD_3V3_LOGIC	SPI3 Chip select 0
36A	X_SPI_RDY	O	VDD_3V3_LOGIC	SPI3 Data ready in master mode
37A	X_SPI_SCLK	O	VDD_3V3_LOGIC	SPI3 Clock
38A	GND	-	Power	Ground 0 V
39A	X_UART_TXD	O	VDD_3V3_LOGIC	Serial transmit signal UART3
40A	X_UART_RTS	O	VDD_3V3_LOGIC	Request to send UART 3
41A	GND	-	Power	Ground 0 V
42A	X_AC97_INT	I/O-	VDD_3V3_LOGIC	I^2S Selection (1 kΩ pull-down (R67) to configure CB or target application for I^2S audio interface)
43A	X_I2S_SDATA_OUT	O	VDD_3V3_LOGIC	I^2S Transmit output (AUD5)
44A	X_I2S_SDATA_IN	I	VDD_3V3_LOGIC	I^2S Receive input (AUD5)
45A	GND	-	Power	Ground 0 V
46A	X_GPIO0/IRQ0	I/O	VDD_3V3_LOGIC	GPIO0/IRQ (µC port GPIO2_24))
47A	X_GPIO2/IRQ/PWM	I/O	VDD_3V3_LOGIC	GPIO2/IRQ/PWM (µC port GPIO4_29)
48A	X_nWKUP	I	VDD_3V3_LOGIC	Wakeup interrupt input (Port P2.1 of CMIC at U17)
49A	GND	-	Power	Ground 0 V
50A	X_CONFIG0	I	VSTBY	Boot-Mode input 0

Table 3: Pinout of the phyCARD-Connector X1, Row A (continued)

Pin Row X1B				
Pin #	Signal	I/O	SL	Description
1B	VDD_3V3	-	Power	3.3 V Primary voltage supply input
2B	VDD_3V3	-	Power	3.3 V Primary voltage supply input
3B	VDD_3V3	-	Power	3.3 V Primary voltage supply input
4B	GND	-	Power	Ground 0 V
5B	VDD_3V3_LOGIC[1]	O	Power	VCC Logic output
6B	VSTBY_IN	-	Power	Standby voltage input
7B	X_nRESET_OUT	-	VDD_3V3_LOGIC	Active low reset output
8B	GND	-	Power	Ground 0 V
9B	X_LVDS_TX1+	O	LVDS	LVDS Chanel 1 positive output
10B	X_LVDS_TX1-	O	LVDS	LVDS Chanel 1 negative output
11B	X_LVDS_TX3+	O	LVDS	LVDS Chanel 3 positive output
12B	X_LVDS_TX3-	O	LVDS	LVDS Chanel 3 negative output
13B	GND	-	Power	Ground 0 V
14B	X_LVDS_CAM_RX+	I	LVDS	Camera data positive input
15B	X_LVDS_CAM_RX-	I	LVDS	Camera data negative input
16B	X_LVDS_CAM_nLOCK	O	LVDS	Camera lock output (active low)
17B	X_I2C_SDA	I/O	VDD_3V3_LOGIC	I^2C2 Data
18B	GND	-	Power	Ground 0 V
19B	X_ETH_LINK	O	VDD_ETH_3V3	Ethernet Link Indicator (open drain)

Table 4: Pinout of the phyCARD-Connector X1, Row B

[1]: Caution! The current draw at VDD_3V3_LOGIC must not exceed 500 mA.

Preliminary

Pin Row X1B				
Pin #	Signal	I/O	SL	Description
20B	X_ETH_RX+	I (O)	VDD_ETH_3V3	Receive positive input (normal) Transmit positive output (reversed)
21B	X_ETH_RX-	I (O)	VDD_ETH_3V3	Receive negative input (normal) Transmit negative output (reversed)
22B	GND	-	Power	Ground 0 V
23B	X_nUSB_HOST_PWR	O	VDD_3V3_LOGIC	USB-HOST1 Power switch output open drain
24B	X_nUSB_HOST_OC	I	VDD_3V3_LOGIC	USB-HOST1 over current input signal
25B	GND	-	Power	Ground 0 V
26B	X_nSUSPEND_TO_RAM	OC	VDD_3V3_LOGIC	Suspend to RAM open collector output (µC port GPIO1_24)
27B	X_USB_HOST_D-	I/O	USB	USB HOST1 transceiver cable interface, D-
28B	X_USB_HOST_D+	I/O	USB	USB HOST1 transceiver cable interface, D+
29B	X_nPOWER_OFF	OC	VDD_3V3_LOGIC	Power Off open collector output (µC port GPIO1_25)
30B	GND	-	Power	Ground 0 V
31B	X_SDIO_D1	I/O	VDD_3V3_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
32B	X_SDIO_D3	I/O	VDD_3V3_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
33B	X_SDIO_CMD	O	VDD_3V3_LOGIC	SD/MMC Command for MMC/SD/SDIO
34B	GND	-	Power	Ground 0 V
35B	X_SPI_CS1	O	VDD_3V3_LOGIC	SPI3 Chip select 1
36B	X_SPI_MOSI	I/O	VDD_3V3_LOGIC	SPI3 Master data out; slave data in
37B	X_SPI_MISO	I/O	VDD_3V3_LOGIC	SPI3 Master data in; slave data out
38B	GND	-	Power	Ground 0 V
39B	X_UART_RXD	I	VDD_3V3_LOGIC	Serial data receive signal UART3
40B	X_UART_CTS	I	VDD_3V3_LOGIC	Clear to send UART3
41B	GND	-	Power	Ground 0 V
42B	X_I2S_BIT_CLK	I/O	VDD_3V3_LOGIC	I^2S Clock (AUD5)
43B	X_I2S_SYNC	O	VDD_3V3_LOGIC	I^2S Frame SYNC (AUD5)
44B	X_I2S_nRESET	O	VDD_3V3_LOGIC	Reset for external I^2S device (connects to GPIO7_12)
45B	GND	-	Power	Ground 0 V
46B	X_SDIO_CD	I	VDD_3V3_LOGIC	SD/MMC Card detect for MMC/SD/SDIO (µC port GPIO5_22)
47B	X_GPIO1/IRQ1	I/O	VDD_3V3_LOGIC	GPIO1/IRQ (µC port GPIO1_06)
48B	X_HW_INTROSPECTION/ GPIO5_26	I/O	VDD_3V3_LOGIC	Hardware introspection interface **for internal use only**
49B	GND	-	Power	Ground 0 V
50B	X_CONFIG1	I	VSTBY	Boot-Mode input 1

Table 4: Pinout of the phyCARD-Connector X1, Row B (continued)

Preliminary

3 Jumpers

For configuration purposes, the phyCARD-i.MX 6 has several solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location of the solder jumpers on the board. *Table 5* provides a functional summary of the solder jumpers which can be changed to adapt the phyCARD-i.MX 6 to your needs. It shows their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable chapter listed in the table.

Note:
Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyCARD-i.MX 6.

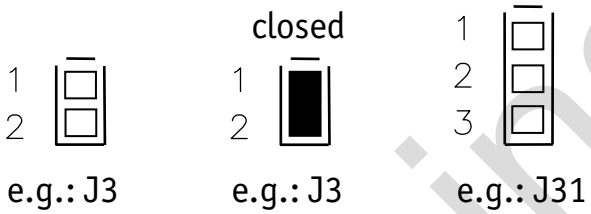

Figure 5: Typical Jumper Pad Numbering Scheme

If manual jumper modification is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Preliminary

Please pay special attention to the "TYPE" column to ensure you are using the correct type of jumper (0 Ω, 10 kΩ, etc...). The jumpers are either 0805 package or 0402 package with a 1/8 W or better power rating.

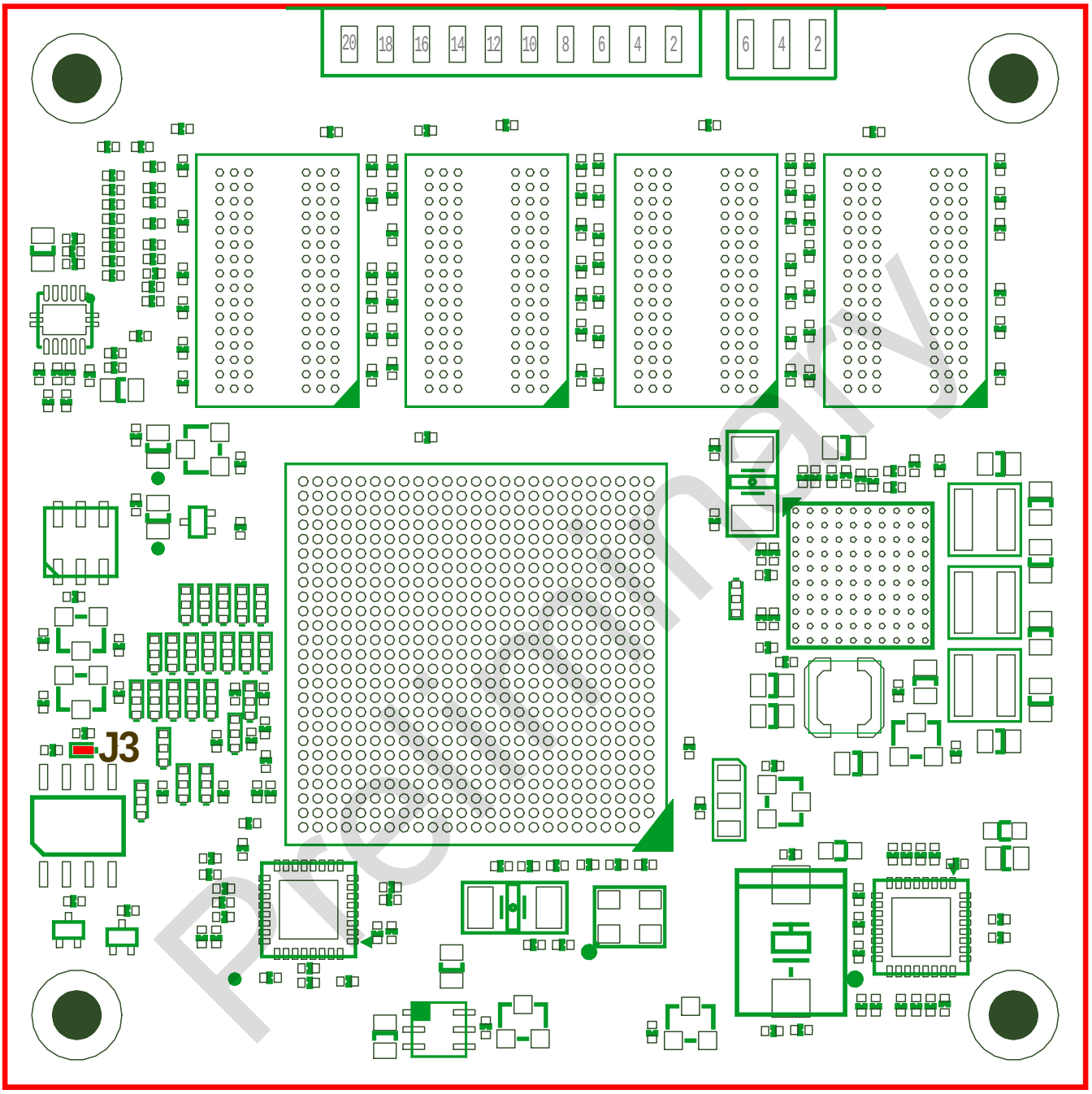

Figure 6: Jumper Locations (top view)

Preliminary

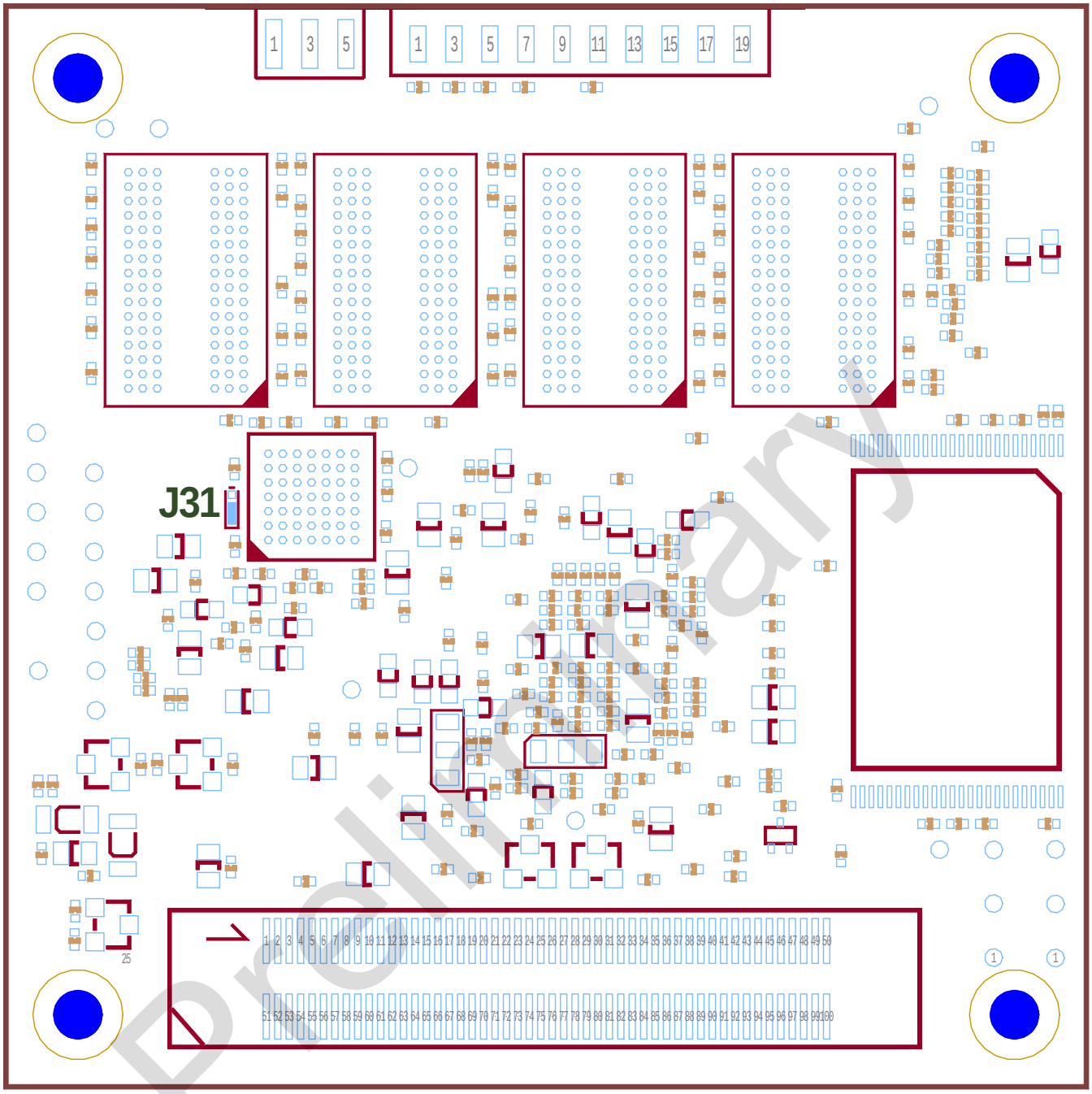

Figure 7: Jumper Locations (bottom view)

The jumpers (J = solder jumper) have the following functions:

Jumper	Description	Type	Chapter
J3	J3 connects the write protect input of the on board EEPROM at U10 with GND. If this jumper is not populated, the EEPROM is write protected.	0R (0402)	*7.3.1*
closed	**EEPROM is not write protected**		
open	EEPROM is write protected. The protection can be changed by the EEPROM_WP/GPIO3_19 signal		
J31	J31 selects rising, or falling edge strobe for the LVDS Deserializer at U27 used for the camera connectivity of the phyCARD-i.MX 6	0R (0402)	*14.1*
2+3	**rising edge strobe used for the LVDS camera signals**		
1+2	falling edge strobe used for the LVDS camera signals		

Table 5: Jumper Settings

Preliminary

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4 Power

The phyCARD-i.MX 6 operates off of a single power supply voltage.

The following sections of this chapter discuss the primary power pins on the phyCARD-Connector X1 in detail.

4.1 Primary System Power (VDD_3V3)

The phyCARD-i.MX 6 operates off of a primary voltage supply with a nominal value of +3.3 V. The on-board power management IC (PMIC) at U29 generates the 2.5 V, 1.375 V, 1.5 V, 0.75 V, 1.2 V and 3.0 V voltage supplies required by the i.MX 6 MCU and on-board components from the primary 3.3 V (VDD_3V3) supplied to the SOM.

For proper operation the phyCARD-i.MX 6 must be supplied with a voltage source of 3.3 V ±5% with 1.5 A load at the VCC pins on the phyCARD-Connector X1.

VDD_3V3: X1 1A, 2A, 3A, 1B, 2B, 3B

Connect all +3.3 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 4A, 8A, 13A, 4B, 8B, 13B

Please refer to *section 2* for information on additional GND Pins located at the phyCARD-Connector X1.

Caution!
As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance all GND pins should be connected to a solid ground plane.

Preliminary

4.2 Backup Voltage (VSTBY)

VSTBY is an additional supply voltage input which has to be connected to a supply voltage of 3.3 V +/- 5% if power management functions will be used. This input voltage supplies the control management IC (CMIC) at U17, which is necessary for all power management functions of the phyCARD module, and the RTC of the power management IC at U29.

To backup the RTC of the power management IC (PMIC) on the module, it is necessary to attach a secondary voltage source of 3.3 V to the phyCARD-i.MX 6 at pin X1B6. This voltage source is supplying the internal backup voltage domain VBACKUP of the PMIC which again supplies the RTC and some critical registers if the primary system power (VDD_3V3) is removed. Applications not requiring a backup mode or power management functions can connect the VSTBY_IN pin to the primary system power supply (VDD = 3.3 V).

4.3 Power Management IC (U29) / Control Management IC (U17)

The phyCARD-i.MX 6 provides a Power Management IC (PMIC) at U29 (DA9063) and a Control Management IC (CMIC) at U17 (MSP430G2153).

Figure 8 presents a graphical depiction of the powering scheme.

4.3.1 Power Management IC (PMIC, U29)

The PMIC at U29 generates the different voltages required by the processor and on-board components, and provides features such as on-chip RTC and different power management functionalities. It is connected to the i.MX 6 via the I^2C bus I2C1. The I2C1 addresses for the PMIC at U29 is 0x58 (page 0 and 1) and 0x59 (page 2 and 3).

Please refer to the dialog SEMICONDUTOR DA9063 datasheet for further information.

4.3.2 Control Management IC (CMIC, U17)

The control management IC at U17 is monitoring the supply voltages and generates necessary control signals for the i.MX 6 processor in respect to the different input signals. It also ensures the correct power sequencing during powering up of the module and configures the boot mode of the i.MX 6 (s. *section 6*).

U17 generates a reset if the on-board voltage generator senses a voltage drop on the primary supply voltage and generates a reset signal, or if a reset is applied at pin X1A7 of the phyCARD-Connector.

Preliminary

4.3.3 Power Domains

The PMIC has two input voltage rails VDD_3V3 and VSTBY_IN as can be seen in *Figure 8*. VDD_3V3 is directly connected to the primary voltage input pins VDD_3V3 of the phyCARD-i.MX 6, whereas VDD_3V3_LOGIC is attached to the primary voltage input pins VDD_3V3 via switch Q17. Q17 is controlled by the PMIC at U29. Not all devices on the phyCARD-i.MX 6 are supplied by the internally generated voltages. Some devices, such as the Ethernet PHY, the LVDS FlatLink™ transmitter, etc. are powered by the primary input voltage VDD_3V3. The following list summarizes the relation between the different voltage rails and the devices on the phyCARD-i.MX 6:

External voltages: VDD_3V3 and VSTBY_IN

Internally generated voltages: VDD_MX6_ARM_1V4 (1.375 V), VDD_MX6_SOC (1.375 V), VDD_3V3_LOGIC (3.3 V), VDD_MX6_SNVS (3.0 V), VDD_HIGH (3.0 V), VDD_DDR3_TERM (1.2V), VDD_DDR3_1V5 (1.5 V), DDR3_VTT (0.75 V), DDR3_VREF (0.75 V).

- VDD_MX6_ARM_1V4: (1.375 V) — i.MX 6 core (VDDARM_IN, VDDARM23_IN)
- VDD_MX6_SOC: (1.375 V) — i.MX 6 SOC (VDDSOC_IN)
- VDD_HIGH: (3.0 V) — i.MX 6 internal regulator (VDDHIGH_IN)
- VDD_MX6_SNVS: (3.0 V) — i.MX 6 backup supply (VDD_SNVS_IN)
- VDD_DDR3_1V5: (1.5 V) — i.MX 6 DDR (NVCC_DRAM), RAM devices supply voltage
- DDR3_VTT: (0.75 V) — RAM devices termination voltage
- DDR3_VREF: (0.75 V) — i.MX 6 DDR3 reference voltage (DRAM_VREF), RAM devices reference voltage
- VDD_3V3_LOGIC: (3.3 V) — i.MX 6 pad supply (NVCC_NANDF, NVCC_JTAG, NVCC_LCD, NVCC_CSI, NVCC_EIM, NVCC_GPIO), I2C EEPROM, SPI Flash, NAND Flash, Camera Deserializer, Ethernet PHY, EMIC
- USB_VBUS (5V) — USB Host/OTG PHY

Preliminary

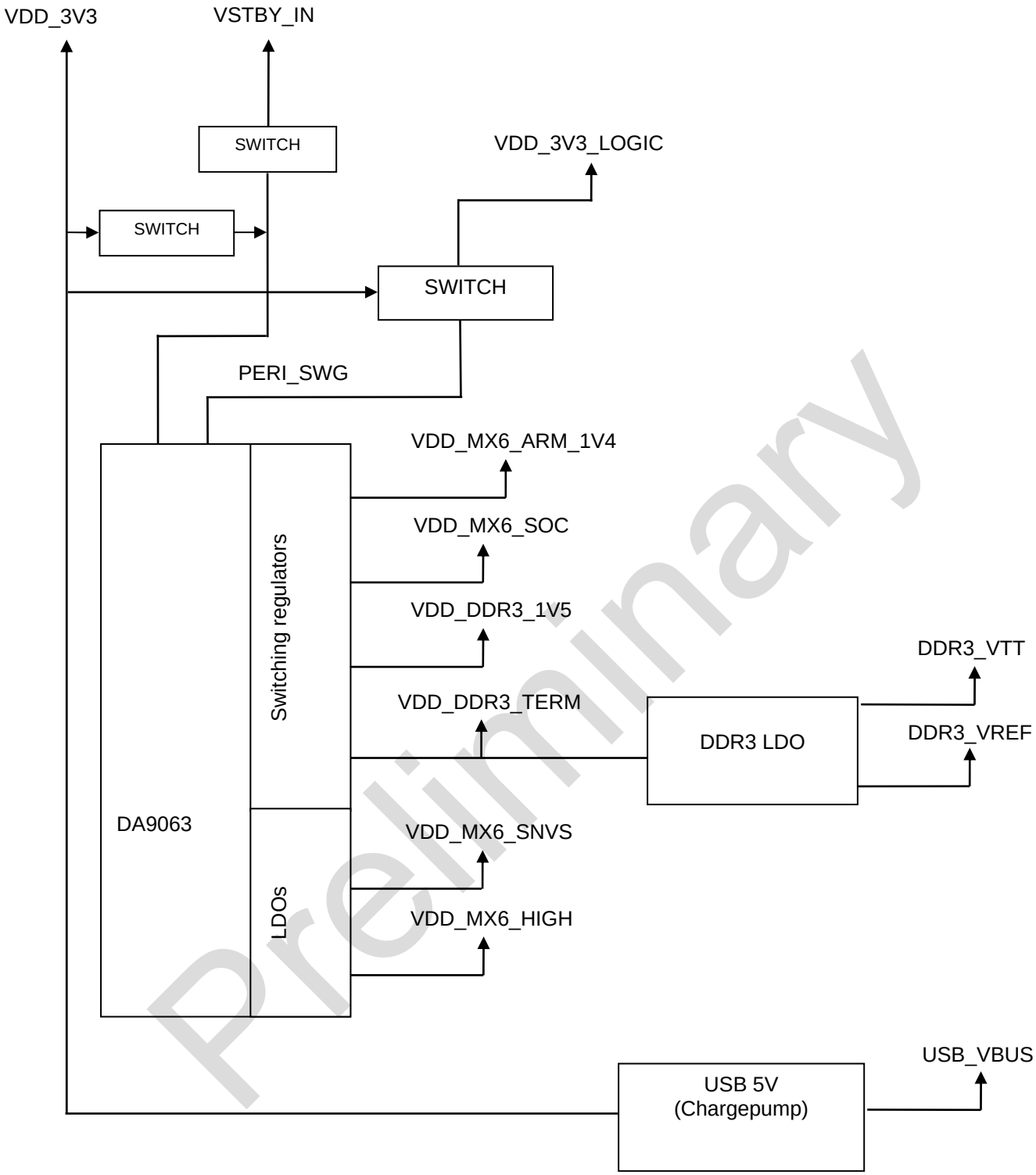

Figure 8: Power Supply Diagram

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4.4 Supply Voltage for external Logic

The voltage level of the phyCARDs logic circuitry is VDD_3V3 (3.3 V) which is derived from the main input voltage VDD_3V3 of the SOM. In order to follow the power-up and power–down sequencing mandatory for the i.MX 6 external devices have to be supplied by the I/O supply voltage VDD_3V3_LOGIC which is brought out at pins X1A5 and X1B5 of the phyCARD-Connector. Use of VDD_3V3_LOGIC ensures that external components are only supplied when the supply voltages of the i.MX 6 are stable.

Caution!
The current draw for VDD_3V3_LOGIC must not exceed 500 mA. If devices with a higher power consumption are to be connected to the phyCARD-i.MX 6 they should be switched on and off by use of VDD_3V3_LOGIC. This way the power-up and power–down sequencing will be considered even if the devices are not supplied directly by VDD_3V3_LOGIC.

If used to control, or supply bus switches on the phyCARD side VDD_3V3_LOGIC also serves to strictly separate the supply voltages generated on the phyCARD-i.MX 6 and the supply voltages used on the carrier board/custom application. That way voltages at the IO pins of the phyCARD-i.MX 6 which are sourced from the supply voltage of peripheral devices attached to the SOM are avoided. These voltages can cause a current flow into the controller especially if peripheral devices attached to the interfaces of the i.MX 6 are supposed to be powered while the phyCARD-i.MX 6 is in suspend mode, or turned off. The bus switches can either be supplied by VDD_3V3_LOGIC on the phyCARD side, or the bus switches' output enable to the SOM can be controlled by VDD_3V3_LOGIC to prevent these voltages from occurring.

Use of VDD_3V3_LOGIC to supply level shifters allows converting the signals according to the needs on the custom target hardware. Alternatively signals can be connected to an open drain circuitry with a pull-up resistor attached to VDD_3V3_LOGIC.

Preliminary

Preliminary

5 Power Management

The phyCARD-i.MX 6 was designed to support applications requiring a power management. Three pins of the X-Arc bus are designated for this purpose. X_nPOWER_OFF and X_nSUSPEND_TO_RAM are output pins which can be used to indicate the power status of the phyCARD-i.MX 6, whereas X_nWKUP is an input pin to apply a wake up signal to the phyCARD-i.MX 6.

The three power management signals are connected to ports of the control management IC (CMIC) at U17. Thus their functionality can be programmed to your needs (refer to *section 4.3.2*).

The following table shows the location of the power management pins on the phyCARD-Connector and the corresponding ports of the CMIC.

Pin #	Signal	I/O	SL	Description
X1A48	X_nWKUP	I	VDD_3V3_LOGIC	Wakeup Interrupt Input (port P2.1 of CMIC at U17)
X1B26	X_nSUSPEND_TO_RAM	OC	VDD_3V3_LOGIC	Suspend to RAM Open Collector Output (port P3.3 of CMIC at U17)
X1B29	X_nPOWER_OFF	OC	VDD_3V3_LOGIC	Power Off Open Collector Output (port P3.2 of CMIC at U17)

Table 6: Power Management Pins

With the two output signals X_nPOWER_OFF (pin X1B29) and X_nSUSPEND_TO_RAM (pin X1B26) three different power states can be defined.

Power State / Signal	Power On	Standby	Off
X_nSUSPEND_TO_RAM	High	Low	X
X_nPOWER_OFF	High	High	Low
VDD_3V3	On	Off	Off
VSTBY	X	On	Off

X=don't care

Table 7: Power States

Please refer to the chapter "Power Management" in the phyCARD Design-In Guide for more information about the implementation of the power management into your design.

Preliminary

Caution!
According to the specification for the phyCARD family writing custom software to utilize pins X_nSUSPEND_TO_RAM and X_nPOWER_OFF requires them to be configured as Open Collector Output.

The power management features of the phyCARD are implemented with the devices at U29 (PMIC) and U17 (CMIC) and allow for a higher granularity in control of the power consumption. To implement power management with the PMIC it can be programmed via an I^2C interface at I^2C address 0x58. Please refer to the *PMIC's User's Guide* for more information.

Preliminary

6 System Configuration and Booting

Although most features of the i.MX 6 microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

The system start-up configuration includes:

- Boot device order configuration

During the reset cycle the operational system boot mode of the i.MX 6 processor is determined by the configuration of two BOOTMODE pins BOOT_MODE[1:0]. These pins select the boot type. If the boot type is set to “Internal boot” (BOOT_MODE[1:0]=10, pins BOOT_CFGx[7:0] are used to configure further boot options. You can find further information about these boot pins in the *i.MX 6 Reference Manual*.

To allow flexible selection of the booting device not all of the BOOT_CFGx[7:0] pins are preconfigured 10 kΩ pull-up, or pull-down configuration resistors, or by jumpers on the phyFLEX-i.MX 6. Some signals are set by the CMIC at U17. During powering up the boot configuration pins X_CONFIG1 and X_XONFIG2 of the module are read by the CMIC. Depending on the setting of these pins the CMIC configures BOOT_MODE[1:0], BOOT_CFG1[7] and BOOT_CFG2[1]. It also ensures the correct power up sequencing so that the i.MX 6 is powered only after the configuration of the boot mode pins. *Table 8* shows the possible settings of pins X_CONFIG1 and X_XONFIG2 and the resulting boot configuration of the i.MX 6. This mechanism provides the possibility to customize the boot behavior by changing the code of the CMIC.

After the i.MX 6 is powered up the internal ROM code is the first code executed during the initialization process of the controller. The ROM code detects which boot devices the controller has to check by using the previously set BOOT_MODE[1:0] and particular BOOT_CFGx[7:0] pin configuration. For serial boot devices, the ROM code polls the communication interface selected, initiates the download of the code into the internal RAM and triggers its execution from there. For memory booting, the ROM code finds the bootstrap in permanent memories such as NAND-Flash or SD-Cards and executes it. Please refer to the *i.MX 6 Reference Manual* for more information.

Preliminary

Boot Mode	X_CONFIG1	X_CONFIG0	Bootsource
0	1	1	NAND
1	1	0	SD0 external
2	0	1	Serial USB OTG (USB0)
3	0	0	Bootconfig from eFUSE

Table 8: Boot Modes of the phyCARD-i.MX 6[1]

The X_CONFIG[1:0] lines have 10 kΩ pull-up resistors populated on the module. Hence leaving the two pins unconnected sets the controller to boot mode 0, NAND boot.

If boot configurations are needed that require change of other boot configuration pins than BOOT_MODE[1:0], BOOT_CFG1[7] and BOOT_CFG2[1] the specific boot settings can also be changed by modifying the resistors and jumpers on the module. Please consider that any change of the default BCFG configuration can also influence other boot modes, which might result in faulty boot behavior.

For further information about the different boot modes and the influence of the BCFG pins please see the *i.MX 6 Reference Manual*.

The following table shows to which level the CMIC sets the different configuration signals for the boot modes. “High-Z” means that the CMIC sets the signal to high impedance, and thus the value of the configuration resistor is used.

Boot Mode	BOOT_MODE [1:0]	BCFG1[7]	BCFG2[1]	Description
0	0b10	1	High-Z	NAND
1	0b10	0	High-Z	SD0
2	0b01	High-Z	High-Z	USB OTG
3	0b00	High-Z	High-Z	eFUSE

Table 9: Boot Configuration Signals generated by the CM

Preliminary

[1]: Default settings are in **bold blue** text

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7 System Memory

The phyCARD-i.MX 6 provides three types of on-board memory:

- 2 Banks DDR3 RAM: 512 MB DDR3 SDRAM (up to 4 GB)[1]
- NAND Flash (VFBGA): 256 MB (up to 4 GB)[1]
- I²C-EEPROM: 4 kB[1]

The following sections of this chapter detail each memory type used on the phyCARD-i.MX 6.

7.1 DDR3 SDRAM (U2-U9)

The RAM memory of the phyCARD-i.MX 6 is comprised of up to two 64 bit wide banks each of four 16-bit wide DDR3-SDRAM chips (Bank 1: U2-U5, Bank 2: U6-U9). The chips are connected to the special DDR interface called Multi Mode DDR Controller (MMDC) of the i.MX 6 processor.

The DDR3 memory is accessed via the second AHB port starting at 0x1000 0000.

Typically the DDR3 SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the i.MX 6 controller. Refer to the *i.MX 6 Reference Manual* for accessing and configuring these registers.

7.2 NAND Flash Memory (U13)

Use of Flash as non-volatile memory on the phyCARD-i.MX 6 provides an easily reprogrammable means of code storage.

These Flash devices are programmable with 3.3 V. No dedicated programming voltage is required.

As of the printing of this manual these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

The NAND Flash memories are connected to the External Interface Module (EIM). /CS0 (NANDF_CS0) of the EIM interface selects the NAND Flash at U13.

Any parts that are footprint (TSOP-48-50-C3) and functionally compatible may be used with the phyCARD-i.MX 6 .

[1]: Please contact PHYTEC for more information about additional module configurations.

Preliminary

7.3 I²C EEPROM (U10)

The phyCARD-i.MX 6 is populated with a non-volatile 4 kB I²C[1] EEPROM at U10. This memory can be used to store configuration data or other general purpose data. This device is accessed through I²C port 1 on the i.MX 6. The control registers for I²C port 1 are mapped between addresses 0x021A 0000 and 0x021A 3FFF. Please see the *i.MX 6 Reference Manual* for detailed information on the registers.

The three lower address bits are fixed to zero which means that the EEPROM can be accessed at I²C address 0x50.

Write protection to the device is accomplished via jumper J3. Refer to *section 7.3.1* for further details on setting this jumper.

7.3.1 EEPROM Write Protection Control (J3)

Jumper J3 controls write access to the EEPROM (U10) device. Closing this jumper allows write access to the device, while removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device.

The following configurations are possible:

EEPROM Write Protection State	J3
Write access allowed	**closed**
Write protected	open

Table 10: EEPROM write protection states via J3[2]

Note: If the jumper is not set, the write protection signal can also be changed by GPIO3_19 of the i.MX 6 controller.

Preliminary

[1]: See the manufacturer's data sheet for interfacing and operation.
[2]: Defaults are in **bold blue** text

8 SD / MMC Card Interfaces

The X-Arc bus features an SD / MMC Card interface. On the phyCARD-i.MX 6 the interface signals extend from the controllers third Ultra Secured Digital (uSDHC3) Host Controller to the phyCARD-Connector. *Table 11* shows the location of the different interface signals on the phyCARD-Connector. The MMC/SD/SDIO Host Controller is fully compatible with the SD Memory Card Specification 3.0 and SD I/O Specification, Part E1, v1.10. The SDC / MMC interface (uSDHC3 of the i.MX 6) of the phyCARD-i.MX 6 supports 4 of the host controller's 8 data channels with a maximum data rate of 104 Mbps (refer to the *i.MX 6 Reference Manual* for more information). The MMC/SD/SDIO Host Controller is supplied by the VDD_3V3_LOGIC voltage, which is derived from the main power supply of the phyCARD-i.MX 6 (3.3 V).

Because of compatibility reasons a card detect signal (X_SDIO_CD) is added to the SD / MMC Card Interface. The card detect function is implemented by using GPIO5_22 of the i.MX 6.

Pin #	Signal	I/O	SL	Description
X1A31	X_SDIO_D0	I/O	VDD_3V3_LOGIC	SD/MMC data bit 0
X1A32	X_SDIO_D2	I/O	VDD_3V3_LOGIC	SD/MMC data bit 2
X1A33	X_SDIO_CLK	O	VDD_3V3_LOGIC	SD/MMC clock for MMC/SD/SDIO0
X1B31	X_SDIO_D1	I/O	VDD_3V3_LOGIC	SD/MMC data bit 1
X1B32	X_SDIO_D3	I/O	VDD_3V3_LOGIC	SD/MMC data bit 3
X1B33	X_SDIO_CMD	I/O	VDD_3V3_LOGIC	SD/MMC command for MMC/SD/SDIO0
X1B46	X_SDIO_CD	I	VDD_3V3_LOGIC	SD/MMC card insertion and extraction detection (GPIO5_22 of the i.MX 6)

Table 11: Location of SD/ MMC Card Interface Signals

Preliminary

Note:
In order to follow the power-up and power–down sequencing mandatory for the i.MX 6 the SD / MMC card interface should be supplied by the I/O supply voltage VDD_3V3_LOGIC which is brought out at pins X1A5 and X1B5 of the phyCARD-Connector. Use of VDD_3V3_LOGIC ensures that the interface is only supplied when the supply voltages of the i.MX 6 are stable.

Caution!
The current draw for VDD_3V3_LOGIC must not exceed 500 mA. If devices with a higher power consumption are to be connected to the GPIOs of the phyCARD-i.MX 6 they should be switched on and off by use of VDD_3V3_LOGIC. This way the power-up and power–down sequencing will be considered even if the devices are not supplied directly by VDD_3V3_LOGIC.

The i.MX 6's requires strict separation of the supply voltages generated on the phyCARD-i.MX 6 and the supply voltages used on the carrier board/custom application. To avoid voltages which are sourced from the supply voltage of the SD / MMC card interface bus switches powered by VDD_3V3_LOGIC on the phyCARD side should be used. Alternatively, the bus switches' output enable to the SOM can be controlled by VDD_3V3_LOGIC (please refer to *section 4.4* for more information).

Please refer to the chapter "SD / MMC" in the phyCARD Design-In Guide for more information about connecting an SD / MMC Card slot to the phyCARD-i.MX 6.

Preliminary

9 Serial Interfaces

The phyCARD-i.MX 6 provides seven serial interfaces some of which are equipped with a transceiver to allow direct connection to external devices:

1. High speed UART (TTL, derived from UART3 of the i.MX 6) with up to 4 MHz and hardware flow control (RTS and CTS signals)
2. High speed USB OTG interface (extended directly from the i.MX 6 USB-HS OTG PHY (USB-PHY))
3. High speed USB HOST interface (extended directly from the i.MX 6 USB HOST PHY (USB-PHY))
4. Auto-MDIX enabled 10/100 Ethernet interface (implemented with an Ethernet PHY attached to the i.MX 6 MII (ENET) interface)
5. I^2C interface (derived from second I^2C port (I2C2) of the i.MX 6)
6. Serial Peripheral Interface (SPI) interface (extended from the third SPI module (eCSPI3) of the i.MX 6)
7. I^2S audio interface Synchronous Serial Interface (SSI5)) (originating from the fifth port of the i.MX 6's Synchronous Serial Interface (SSI5))

The following sections of this chapter detail each of these serial interfaces and any applicable configuration jumpers.

Caution!
The i.MX 6's power sequencing requires strict separation of the supply voltages generated on the phyCARD-i.MX 6 and the supply voltages used on the carrier board/custom application. Especially if peripheral devices attached to the interfaces of the i.MX 6 are supposed to be powered while the phyCARD-i.MX 6 is in suspend mode, or turned off. This situation might result in voltages at the IO pins of the phyCARD-i.MX 6 which are sourced from the supply voltage of the peripheral device, and which cause a current flow into the controller. To avoid these voltages bus switches powered by VDD_3V3_LOGIC on the phyCARD side should be used. Alternatively, the bus switches' output enable to the SOM can be controlled by VDD_3V3_LOGIC.

Please refer to the phyCARD Design-In Guide (LAN-051) for more information about using the serial interfaces of the phyCARD-i.MX 6 in customer applications.

Preliminary

9.1 Universal Asynchronous Interface

The phyCARD-i.MX 6 provides a high speed universal asynchronous interface with up to 4 MHz and hardware flow control (RTS and CTS signals). The following table shows the location of the signals on the phyCARD-Connector.

Pin #	Signal	I/O	SL	Description
X1A39	X_UART_TXD	O	VDD_3V3_LOGIC	Serial data transmit signal UART 3
X1A40	X_UART_RTS	O	VDD_3V3_LOGIC	Request to send UART 3
X1B39	X_UART_RXD	I	VDD_3V3_LOGIC	Serial data receive signal UART 3
X1B40	X_UART_CTS	I	VDD_3V3_LOGIC	Clear to send UART 3

Table 12: Location of the UART Signals

The signals extend from UART3 of the i.MX 6 directly to the phyCARD-Connector without conversion to RS-232 level. External RS-232 transceivers must be attached by the user if RS-232 levels are required.

9.2 USB OTG Interface

The phyCARD-i.MX 6 provides a high speed USB OTG interface which uses the i.MX 6 embedded HS USB OTG PHY.

Because of the processor is not featuring the USB over current detection GPIO1_20 can be used as USB-OTG over current input signal. The signal is active low.

For self-powered devices an external USB Standard-A (for USB host), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyCARD-i.MX 6 USB OTG functionality. To attach devices which require the VBUS supply voltage an external power logic (or charge pump) capable of sourcing 5 V power must be provided on the carrier board. Signal X_nUSB_OTG_PWR (X1A23) allows control of the external power logic. After reset signal X_nUSB_OTG_PWR is low (meaning active). Therefore an external power switch is enabled and booting via USB is possible.

The applicable interface signals can be found on the phyCARD-Connector as shown in *Table* 13.

Preliminary

Pin #	Signal	I/O	SL	Description
X1A23	X_nUSB_OTG_PWR	O	VDD_3V3_LOGIC	USB OTG power switch output open drain, low active
X1A24	X_nUSB_OTG_OC	I	VDD_3V3_LOGIC	USB OTG over current input signal, low active
X1A26	X_USB_VBUS	I	5V	USB VBUS voltage
X1A27	X_USB_DM	I/O		USB transceiver cable interface, D-
X1A28	X_USB_DP	I/O		USB transceiver cable interface, D+
X1A29	X_USB_UID	I		USB on the go transceiver cable ID resistor connection

Table 13: Location of the USB OTG Signals

In order to use the phyCARD-i.MX 6 as USB device an USB Standard-B connector) and an appropriate configuration of the ID pin on the carrier board is all that is needed.

9.3 USB Host Interface

The i.MX 6 provides a high speed USB Host interface which uses the i.MX 6 embedded HS USB Host PHY.
Neither VBUS detection, nor the ID pin is required. Therefore USB_VBUS and ID are not brought out to the phyCARD-Connector.

For self-powered devices an external USB Standard-A (for USB Host) connector is all that is needed to interface the phyCARD-i.MX 6 USB Host functionality. To attach devices which require the VBUS supply voltage an external power logic (or charge pump) capable of sourcing 5 V power must be provided on the carrier board. Signal X_nUSB_HOST_ PWR (X1B23) allows control of the external power logic. It can be used to switch an external VBUS power supply and is derived from the USB HOST interface of the i.MX 6.

The applicable interface signals (D+/D-/ PWR/OC) can be found on the phyCARD-Connector as shown in the following table.

Pin #	Signal	I/O	SL	Description
X1B23	X_nUSB_HOST_PWR	O	VDD_3V3_LOGIC	USB-HOST power switch output open drain
X1B24	X_nUSB_HOST_OC	I	VDD_3V3_LOGIC	USB-HOST over current input signal
X1B27	X_USB_HOST_D-	I/O		USB HOST transceiver cable interface, D-
X1B28	X_USB_HOST_D+	I/O		USB HOST transceiver cable interface, D+

Table 14: Location of the USB-Host Signals

Preliminary

9.4 Ethernet Interface

Connection of the phyCARD-i.MX 6 to the world wide web or a local area network (LAN) is possible using the on-board PHY at U11. It is connected to the MII interface of the i.MX 6. The FEC operates with a data transmission speed of 10 Mbit/s or 100 Mbit/s.

9.4.1 Ethernet PHY (U11)

With an Ethernet PHY mounted at U11 the phyCARD-i.MX 6 has been designed for use in 10Base-T and 100Base-T networks. The 10/100Base-T interface with its LED signals extends to phyCARD-Connector X1.

Pin #	Signal	I/O	SL	Description
X1A19	X_ETH_SPEED	O	VCC_3V3	Ethernet Speed Indicator (Open Drain)
X1A20	X_ETH_TX+	O (I)	VCC_3V3	Transmit positive output (normal) Receive positive input (reversed)
X1A21	X_ETH_TX-	O (I)	VCC_3V3	Transmit negative output (normal) Receive negative input (reversed)
X1B19	X_ETH_LINK	O	VCC_3V3	Ethernet Link Indicator (Open Drain)
X1B20	X_ETH_RX+	I (O)	VCC_3V3	Receive positive input (normal) Transmit positive output (reversed)
X1B21	X_ETH_RX-	I (O)	VCC_3V3	Receive negative input (normal) Transmit negative output (reversed)

Table 15: Location of the Ethernet Signals

The Ethernet transceiver supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet controller also features an Auto-negotiation to automatically determine the best speed and duplex mode.

The Ethernet transceiver is directly connected to the MII Interface of the i.MX 6. Please refer to the *i.MX 6 Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100Base-T network some external circuitry is required. The required 49.9 Ω +/-1% termination resistors on the analog signals (ETH_RX±, ETH_TX±) are already populated on the module. Connection to an external Ethernet magnetics should be done using very short signal traces. The TPI+/TPI- and TPO+/TPO- signals should be routed as 100 Ω differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

An example for the external circuitry is shown in the phyCARD's Design Guide.

Preliminary

If you are using the applicable carrier board for the phyCARD-i.MX 6 (part number PBA-A-03), the external circuitry mentioned above is already integrated on the board (refer to *section 17.3.4*).

Caution!
Please see the datasheet of the Ethernet transceiver as well as the phyCARD's Design Guide (LAN-051) when designing the Ethernet transformer circuitry.

The reset input of the Ethernet controller is permanently connected to the reset output signal POR_B of the control management IC U17 on the phyCARD-i.MX 6 (refer to *section 4.3.2*).

9.4.2 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCARD-i.MX 6 is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

9.5 I^2C Interface

The Inter-Integrated Circuit (I^2C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The i.MX 6 contains three identical and independent multimaster Fast mode I^2C modules. The interface of the third module (I2C3) extends directly to the phyCARD-Connector. No other components are connected to this I^2C module. The following table lists the I^2C port on the phyCARD-Connector:

Pin #	Signal	I/O	SL	Description
X1A17	X_I2C_SCL	O	VDD_3V3_LOGIC	I^2C Clock Output
X1B17	X_I2C_SDA	I/O	VDD_3V3_LOGIC	I^2C Data

Table 16: I^2C Interface Signal Location

Preliminary

9.6 SPI Interface

The Serial Peripheral Interface (SPI) interface is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. 6 pins of the X-Arc bus are designated to the SPI interface (refer to *Table 2*). In addition to the four standard signals a second chip select and the SPI ready signal are provided at the X-Arc bus. The later signal allows to also use SPI devices with "5-wire protocol". The Enhanced Configurable SPI (ECSPI) of the i.MX 6 has five separate modules (ECSPI1 to ECSPI5). The interface signals of the third module (ECSPI3) are made available on the phyCARD-Connector. This module is Master/Slave configurable.

The i.MX 6 does not provide the SPI ready signal. Because of that an additional GPIO (GPIO1_9) is attached to pin X1A36 instead. The following table lists the SPI signals on the phyCARD-Connector:

Pin #	Signal	I/O	SL	Description
X1A35	X_SPI0_CS0	O	VDD_3V3_LOGIC	ECSPI3 Chip select 0
X1B35	X_SPI0_CS1	O	VDD_3V3_LOGIC	ECSPI3 Chip select 1
X1A36	X_SPI0_RDY	O	VDD_3V3_LOGIC	SPI Ready signal implemented by use of GPIO1_9
X1A37	X_SPI0_CLK	O	VDD_3V3_LOGIC	ECSPI3 clock
X1B36	X_SPI0_MOSI	I/O	VDD_3V3_LOGIC	ECSPI3 Master data out; slave data in
X1B37	X_SPI0_MISO	I/O	VDD_3V3_LOGIC	ECSPI3 Master data in; slave data out

Table 17: SPI Interface Signal Location

9.7 I²S Audio Interface (SSI)

The Synchronous Serial Interface (SSI) of the phyCARD-i.MX 6 is a full-duplex, serial interface that allows to communicate with a variety of serial devices, such as standard codecs, digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I^2S) and Intel AC'97 standard. The i.MX 6 provides three instances of the SSI module. On the phyCARD-i.MX 6 SSI5 is brought out to the phyCARD -Connector.

With reference to the X-Arc bus specification, the main purpose of this interface is to connect to an external codec, such as I^2S. Four signals extend from the i.MX 6 SSI module to the phyCARD-Connector (I2S_BIT_CLK, I2S_SYNC, I2S_SDATA_OUT, I2S_SDATA_IN). X_ AC97_INT and X_I2S_nRESET are two additional pins assisting the functionality of this interface. X_ AC97_INT is used as input and output. As output it signals which codec is supported by the phyCARD. Use of this pin as an input enables to attach an external interrupt to GPIO (GPIO5_14). X_I2S_nRESET is connected to GPIO7_12 of the i.MX 6 allowing to perform a software reset for the device attached to the interface.

Preliminary

Please also read the phyCARD Design-In Guide for more information about how to use the I^2S interface.

Pin #	Signal	I/O	SL	Description
X1A42	X_AC97_INT	I/O	VDD_3V3_LOGIC	I^2S Interrupt Input (connected to GPIO5_14)
X1A43	X_I2S_SDATA_OUT	O	VDD_3V3_LOGIC	I^2S Transmit Output
X1A44	X_I2S_SDATA_IN	I	VDD_3V3_LOGIC	I^2S Receive Input
X1B42	X_I2S_BIT_CLK	I	VDD_3V3_LOGIC	I^2S Transmit Clock
X1B43	X_I2S_SYNC	O	VDD_3V3_LOGIC	I^2S Transmit Frame Sync
X1B44	X_I2S_nRESET	O	VDD_3V3_LOGIC	Reset for external I^2S device (derived from GPIO7_12)

Table 18: SSI Interface Signal Location

Preliminary

10 General Purpose I/Os

The X-Arc bus provides 3 GPIO / IRQ signals. *Table 19* shows the location of the GPIO / IRQ pins on the phyCARD-Connector, as well as the corresponding ports of the i.MX 6.

Pin #	Signal	I/O	SL	Description
X1A46	X_GPIO0/IRQ0	I/O	VDD_3V3_LOGIC	General purpose input/output 0 (GPIO2_24 of i.MX 6)
X1A47	X_GPIO2/IRQ/PWM	I/O	VDD_3V3_LOGIC	General purpose input/output 2 (GPIO4_29 of i.MX 6)
X1B47	X_GPIO1/IRQ1	I/O	VDD_3V3_LOGIC	General purpose input/output 1 (GPIO1_6 of i.MX 6)

Table 19: Location of GPIO and IRQ pins

As can be seen in the table above the voltage level is VDD_3V3_LOGIC, which is 3.3 V. In other words VDD_3V3_LOGIC is identical with the supply voltage of the phyCARD-i.MX 6. But in order to follow the power-up and power–down sequencing mandatory for the i.MX 6 VDD_3V3_LOGIC is switched on with a certain delay. Because of that use of VDD_3V3_LOGIC ensures that external components are only supplied when the supply voltages of the i.MX 6 are stable. External devices connected to the GPIO pins should be supplied by VDD_3V3_LOGIC available at X1A5 and X1B5 (refer to *section 4.4*). Alternatively an open drain circuit with a pull-up resistor attached to VDD_3V3_LOGIC can be connected to the GPIOs of the phyCARD-i.MX 6.

Caution!
The current draw for VDD_3V3_LOGIC must not exceed 500 mA. If devices with a higher power consumption are to be connected to the GPIOs of the phyCARD-i.MX 6 they should be switched on and off by use of VDD_3V3_LOGIC. This way the power-up and power–down sequencing will be considered even if the devices are not supplied directly by VDD_3V3_LOGIC.

Caution!
The i.MX 6's requires strict separation of the supply voltages generated on the phyCARD-i.MX 6 and the supply voltages used on the carrier board/custom application. To avoid voltages which are sourced from the supply voltage of peripheral devices attached to the GPIOs bus switches powered by VDD_3V3_LOGIC on the phyCARD side should be used. Alternatively, the bus switches' output enable to the SOM can be controlled by VDD_3V3_LOGIC (please refer to *section 4.4* for more information).

Please refer to the chapter "GPIOs" in the phyCARD Design-In Guide for more information about how to integrate the GPIO pins in your design.

Preliminary

11 User LEDs

The phyFLEX-i.MX 6 provides two user LEDs on board, a red (D2) and a green (D1). D2 can be controlled by setting GPIO3_20 (pad EIM_D20) and D1 can by controlled by setting GPIO1_7 (pad GPIO_7) to the desired output level. A high-level turns the LED on, a low-level turns it off.

Preliminary

12 Debug Interface (X3))

The phyCARD-i.MX 6 is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends to a 2.54 mm pitch contact pad row at X3 which allows for attaching a 2x10 pin, 2.54 mm pitch pin header on the edge of the module PCB. *Figure 9* and *Figure 10* show the position of the debug interface (JTAG connector X3, DEBUG INTERFACE X2) on the phyCARD-i.MX 6 module. Software debugging via DEBUG INTERFACE connector X2 requires special tools (hardware/software). For further information please see the *i.MX 6 Reference Manual*.

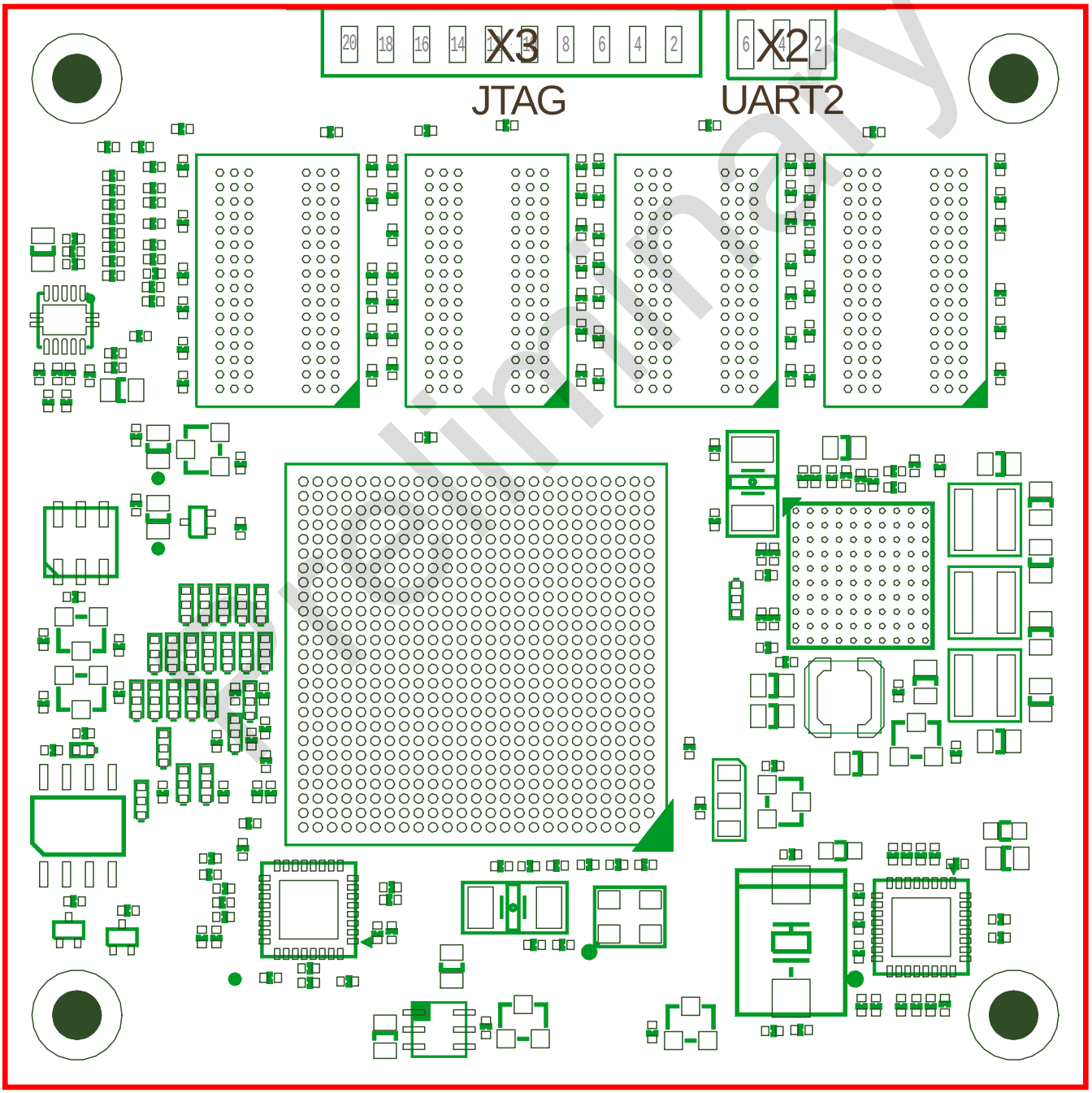

Figure 9: JTAG Interface at X2 and X3 (top view)

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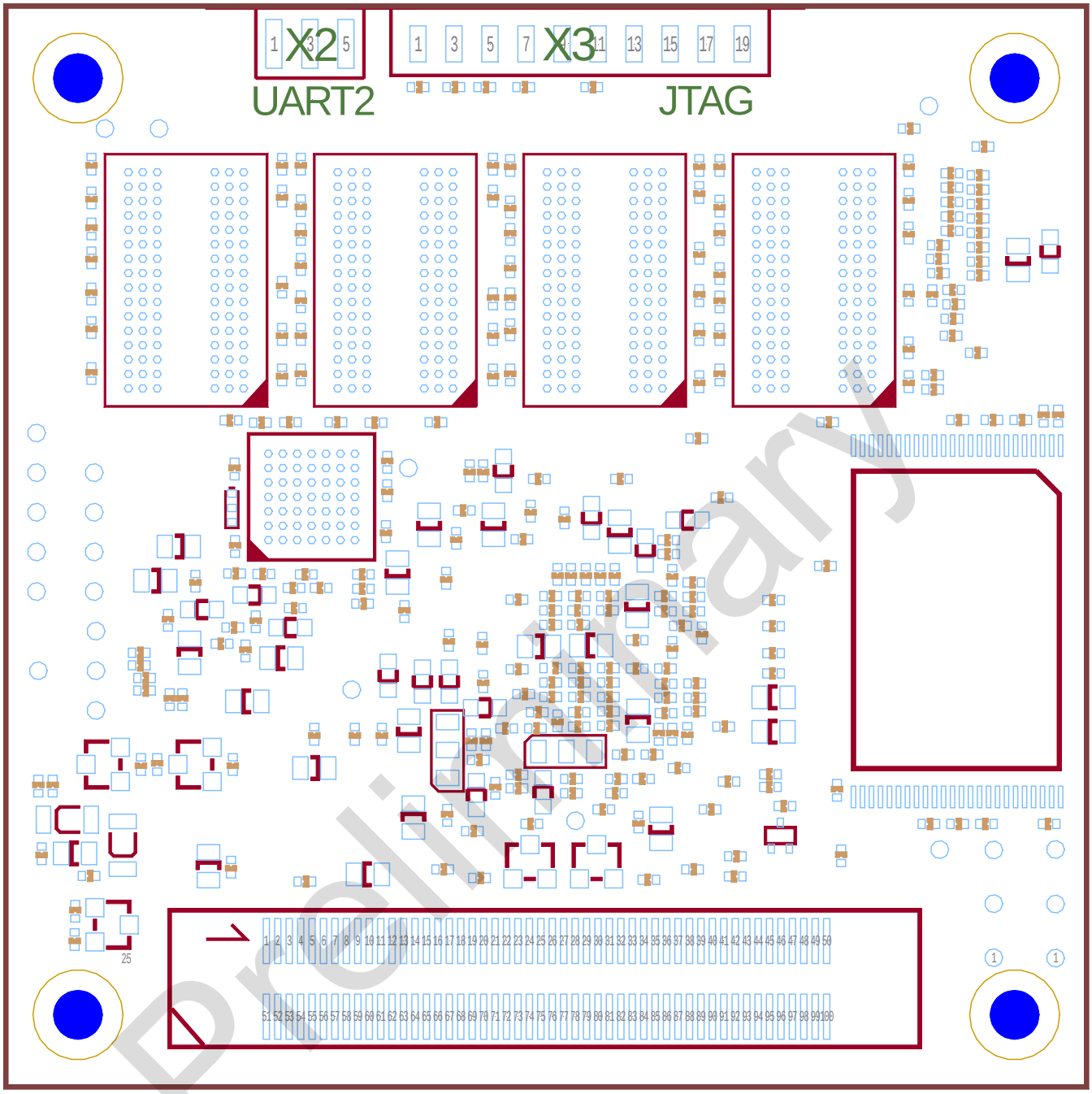


Figure 10: JTAG Interface at X2 and X3 (bottom view)

Pin 1 of the JTAG connector X3 is on the connector side of the module. Pin 2 of the JTAG connector is on the controller side of the module.

Note:
The connectors X2 and X3 only populates phyCARD-i.MX 6 modules with a special order code. DEBUG/JTAG connectors X2 and X3 are not populated on the standard phyCARD module. We recommend integration of a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface.

See the following table for details on the JTAG signal pin assignment (X3).

Signal	Pin Row*		Signal
	A	B	
VSUPPLY (VDD_3V3_LOGIC)	2	1	TREF (VDD_3V3_LOGIC via 0 Ω)
GND	4	3	X_JTAG_TRSTB (10 kΩ pull-up)
GND	6	5	X_JTAG_TDI (10 kΩ pull-up)
GND	8	7	X_JTAG_TMS (10 kΩ pull-up)
GND	10	9	X_JTAG_TCK
GND	12	11	Connected to X_JTAG_TCK via 0 Ω
GND	14	13	X_JTAG_TDO
GND	16	15	X_nRESET_IN
GND	18	17	NC
GND	20	19	NC

Table 20: JTAG Connector X3 Signal Assignment

***Note:** Row A is on the controller side of the module and row B is on the connector side of the module

The following table shows details on the debug interface pin assignment (X2).

Signal	Pin Row*		Signal
	A	B	
VDD_3V3	2	1	GND
VDD_3V3_LOGIC	4	3	UART2_TX
GND	6	5	UART2_RX

Table 21: Debug interface Connector X2 Signal Assignment

Preliminary

13 LVDS Display Interface

The LVDS-Signals from channel serializer #0 of the i.MX 6's on-chip LVDS Display Bridge (LDB) are brought out at the X-Arc Connector X1. Thus an LVDS-Display can connect directly to the phyCARD-i.MX 6. The location of the applicable interface signals (X_LVDS_TX0-3+, X_LVDS_TX0-3-, X_LVDS_TXCLK+ and X_LVDS_TXCLK-) can be found in the table below.

Pin #	Signal	I/O	SL	Description
X1A9	X_LVDS_TX0+	O	LVDS	LVDS0 data0+
X1A10	X_LVDS_TX0-	O	LVDS	LVDS0 data0-
X1A11	X_LVDS_TX2+	O	LVDS	LVDS0 data2+
X1A12	X_LVDS_TX2-	O	LVDS	LVDS0 data2-
X1A14	X_LVDS_TXCLK+	O	LVDS	LVDS0 clock+
X1A15	X_LVDS_TXCLK-	O	LVDS	LVDS0 clock-
X1B9	X_LVDS_TX1+	O	LVDS	LVDS0 data1+
X1B10	X_LVDS_TX1-	O	LVDS	LVDS0 data1-
X1B11	X_LVDS_TX3+	O	LVDS	LVDS0 data3+
X1B12	X_LVDS_TX3-	O	LVDS	LVDS0 data3-

Table 22: Display Interface Signal Location

13.1 LVDS Display Interface pixel mapping

The phyCARD specification defines the pixel mapping of the LVDS display interface. The pixel mapping equates to the OpenLDI respectively Intel 24.0 standard. Thus you can connect 18-bit as well as 24-bit LVDS displays to the phyCARD. *Table 23* and *Table 24* show the recommended pixel mapping of the LVDS display. For further information please see the phyCARD Design Guide.

Note:
Make sure that the LVDS display you want to use provides the same pin mapping as the phyCARD. Normally this is only important for 24-bit LVDS displays because due to the organization of the LVDS pixel mapping all common 18-bit LVDS displays should work.

Preliminary

18-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G0	R5	R4	R3	R2	R1	R0
A1	B1	B0	G5	G4	G3	G2	G1
A2	DE	VSYNC	HSYNC	B5	B4	B3	B2
A3	0	0	0	0	0	0	0

Table 23: Pixel Mapping of 18-bit LVDS Display Interface

24-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G2	R7	R6	R5	R4	R3	R2
A1	B3	B2	G7	G6	G5	G4	G3
A2	DE	VSYNC	HSYNC	B7	B6	B5	B4
A3	0	B1	B0	G1	G0	R1	R0

Table 24: Pixel Mapping of 24-bit LVDS Display Interface

Preliminary

14 LVDS Camera Interface

The phyCARD-i.MX 6 uses one 10-Bit LVDS Random Lock Deserializer (U27) to receive LVDS-Signals from a LVDS Camera Interface (1-channel). The LVDS Deserializer converts the LVDS Signals to a 10-bit wide parallel data bus and separate clock which can be used as inputs for the i.MX 6 Camera Sensor Interfaces (U27 is connected to CSI0). The 10-bit wide data bus consists of 8 color information bits and 2 sync bits (HSYNC/VSYNC).

The following table shows the location of the applicable interface signals on the phyCARD - Connector.

Pin #	Signal	ST	Voltage Domain	Description
X1A16	X_LVDS_CAM_MCLK	O	VDD_3V3_LOGIC	Camera master clock
X1B14	X_LVDS_CAM_RX+	LVDS_I	VDD_3V3_LOGIC	Camera data+
X1B15	X_LVDS_CAM_RX-	LVDS_I	VDD_3V3_LOGIC	Camera0 data-
X1B16	X_LVDS_CAM_nLOCK	O	VDD_3V3_LOGIC	LOCK output of the Deserializer at U27

Table 25: Camera Interface Signal Location at X1

To assists the implementation of a power management the Deserializer's REN input is connected to the CSI0_DATA_EN signal (P3) of the i.MX 6. Furthermore the nPWRDN signal of the Deserializer is connected to CAM_LVDS_PRWDN/GPIO5_27 (N5) of the i.MX 6. Thereby the LVDS Deserializer can be turned off by software.

14.1 Signal Configuration (J31)

J31 selects rising, or falling edge strobe for the LVDS Deserializer at U27 used for the camera connectivity of the phyCARD-i.MX 6 CSI0 port.

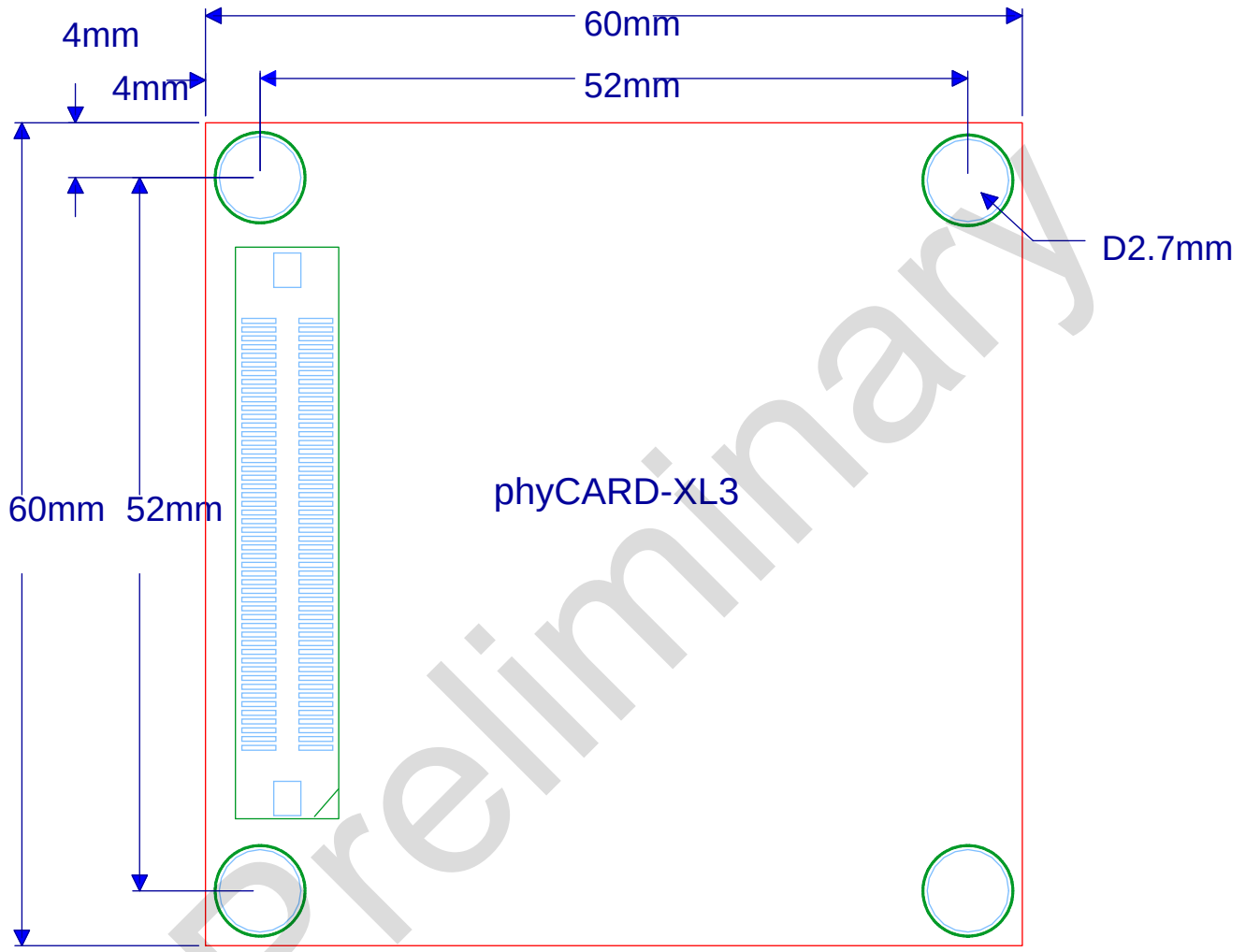
Position	Description	Type
2+3	**rising edge strobe used for the LVDS camera signals**	0R (0402)
1+2	falling edge strobe used for the LVDS camera signals	

Table 26: LVDS Signal Configuration J31

Preliminary

15 Technical Specifications

The physical dimensions of the phyCARD-i.MX 6 are represented in *Figure 11*. The module's profile is max. 11.4 mm thick, with a maximum component height of 5.0 mm on the bottom (connector) side of the PCB and approximately 3.0 mm on the top (microcontroller) side. The board itself is approximately 1.4 mm thick.



Preliminary

Figure 11: Physical Dimensions

Note:
To facilitate the integration of the phyCARD-i.MX 6 into your design, the footprint of the phyCARD-i.MX 6 is available for download (see *section 16.1*).

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Additional specifications:

Dimensions:	60 mm x 60 mm
Weight:	approximately 16 g with all optional components mounted on the circuit board
Storage temperature:	-40 °C to +125 °C
Operating temperature:	0 °C to +70 °C (commercial) -40 °C to +80 °C (industrial)
Humidity:	95% r.F. not condensed
Operating voltage:	VCC 3.3 V
Power consumption: Supply voltage: Condition hardware: Condition software / commands executed	Max. 2.2 W VCC = 3.3 V, VSTBY = 0 V, 256 MB LP-DDR-RAM, 512 MB NAND Flash, Ethernet, 720 MHz CPU frequency at 20 °C Linux; seriell and Ethernet communication + dd + fbtest

These specifications describe the standard configuration of the phyCARD-i.MX 6 as of the printing of this manual.

Preliminary

Connectors on the phyCARD:

Manufacturer	Molex
Number of pins per contact rows	100 (2 rows of 50 pins each)
Molex part number (lead free)	52885-1074 (receptacle)

Matting connectors on the phyBASE:

Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	100 (2 rows of 50 pins each)
Molex part number (lead free)	55091-1075/1074 (header)
PHYTEC part number (lead free)	VB090

Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	100 (2 rows of 50 pins each)
Molex part number (lead free)	53553-1079 (header)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCARD—i.MX 6. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (3 mm) on the bottom side of the phyCARD must be subtracted.

Please refer to the corresponding data sheets and mechanical specifications provided by Molex (*www.molex.com*).

Preliminary

Preliminary

16 Hints for Integrating and Handling the phyCARD-i.MX 6

16.1 Integrating the phyCARD-i.MX 6

Besides this hardware manual much information is available to facilitate the integration of the phyCARD-i.MX 6 into customer applications.

1. the design of the standard phyCARD Carrier Board can be used as a reference for any customer application
2. many answers to common questions can be found at http://www.phytec.de/de/support/faq/faq-phyCARD-i.MX 6.html, or http://www.phytec.eu/europe/support/faq/faq-phyCARD-i.MX 6.html.
3. a Design-In Guide can be downloaded from the same web side. It provides recommendations as to development of customized carrier board target hardware in which the phyCARD-i.MX 6 (and other phyCARDs) can be deployed.
4. the link "Carrier Board" within the category Dimensional Drawing leads to the layout data as shown in *Figure 12*. It is available in different file formats.
5. different support packages are available to support you in all stages of your embedded development. Please visit http://www.phytec.de/de/support/support-pakete.html, or http://www.phytec.eu/europe/support/support-packages.html, or contact our sales team for more details.

Preliminary

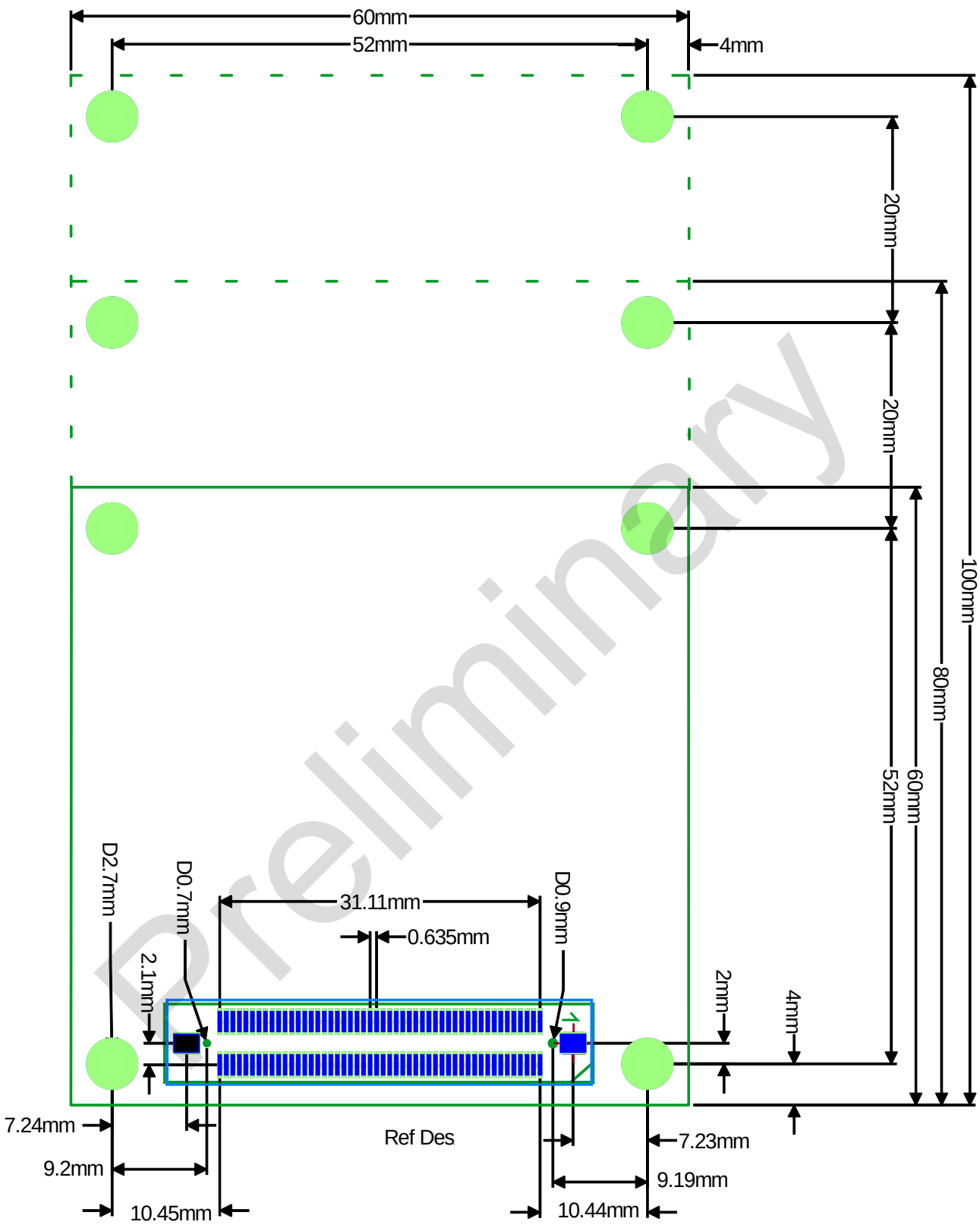

Figure 12: Footprint of the phyCARD-i.MX 6

16.2 Handling the phyCARD-i.MX 6

- **Modifications on the phyCARD Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCARD into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCARD module. As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance all GND pins should be connected to a solid ground plane.

Note!
Please refer to the phyCARD Design-In Guide (LAN-051) for additional information, layout recommendations and example circuitry.

Preliminary

Preliminary

17 The phyCARD-i.MX 6 on the phyBASE

PHYTEC phyBASE Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC System on Module (SOM) modules. phyBASE Boards are designed for evaluation, testing and prototyping of PHYTEC System on Module in laboratory environments prior to their use in customer designed applications.

The phyCARD-i.MX 6 Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCARD-i.MX 6 System on Module. The carrier board design allows easy connection of additional extension boards featuring various functions that support fast and convenient prototyping and software evaluation.

The phyBASE supports the following features for the phyCARD-i.MX 6 modules:

- Power supply circuits to supply the modules and the peripheral devices
- Support of different power modes of appropriate phyCARD
- Full featured 4 line RS-232 transceiver supporting data rates of up to 120 kbps, hardware handshake and RS-232 connector
- Seven USB-Host interfaces
- USB-OTG interface
- 10/100 Mbps Ethernet interface
- Complete audio and touch screen interface
- LVDS display interface with separate connectors for data lines and display / backlight supply voltage
- Circuitry to allow dimming of a backlight
- Secure Digital Card / Multi Media Card Interface
- Two extension connectors for PHYTEC Extension Boards (PEBs) or customer prototyping purposes featuring one USB, one I^2C and one SPI interface, as well as one GPIO/IRQ at either connector
- DIP-Switch to configure various interface options
- Jumper to configure the boot options for the phyCARD-i.MX 6 module mounted
- RTC with battery supply/backup

Preliminary

17.1 Concept of the phyBASE Board

The phyCARD Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCARD System on Module. The carrier board design allows easy connection of additional extension boards featuring various functions that support fast and convenient prototyping and software evaluation. The carrier board is compatible with all phyCARDs.

This modular development platform concept includes the following components:

- the **phyCARD-i.MX 6 module** populated with the i.MX 6 processor and all applicable SOM circuitry such as DDR SDRAM, Flash, PHYs, and transceivers to name a few.

- the **phyBASE** which offers all essential components and connectors for start-up including: a power socket which enables connection to an **external power adapter**, interface connectors such as **DB-9**, **USB** and **Ethernet** allowing for use of the SOM's interfaces with standard cable.

The following sections contain specific information relevant to the operation of the phyCARD-i.MX 6 mounted on the phyCARD Carrier Board.

Note:
Only features of the phyBASE which are supported by the phyCARD-i.MX 6 are described. Jumper settings and configurations which are not suitable for the phyCARD-i.MX 6 are not described in the following chapters.

Preliminary

17.2 Overview of the phyBASE Peripherals

äThe phyBASE is depicted in *Figure 13*. It is equipped with the components and peripherals listed in *Table 27*, *Table 28*, *Table 29* and *Table 30*. For a more detailed description of each peripheral refer to the appropriate chapter listed in the applicable table. *Figure 13* highlights the location of each peripheral for easy identification.

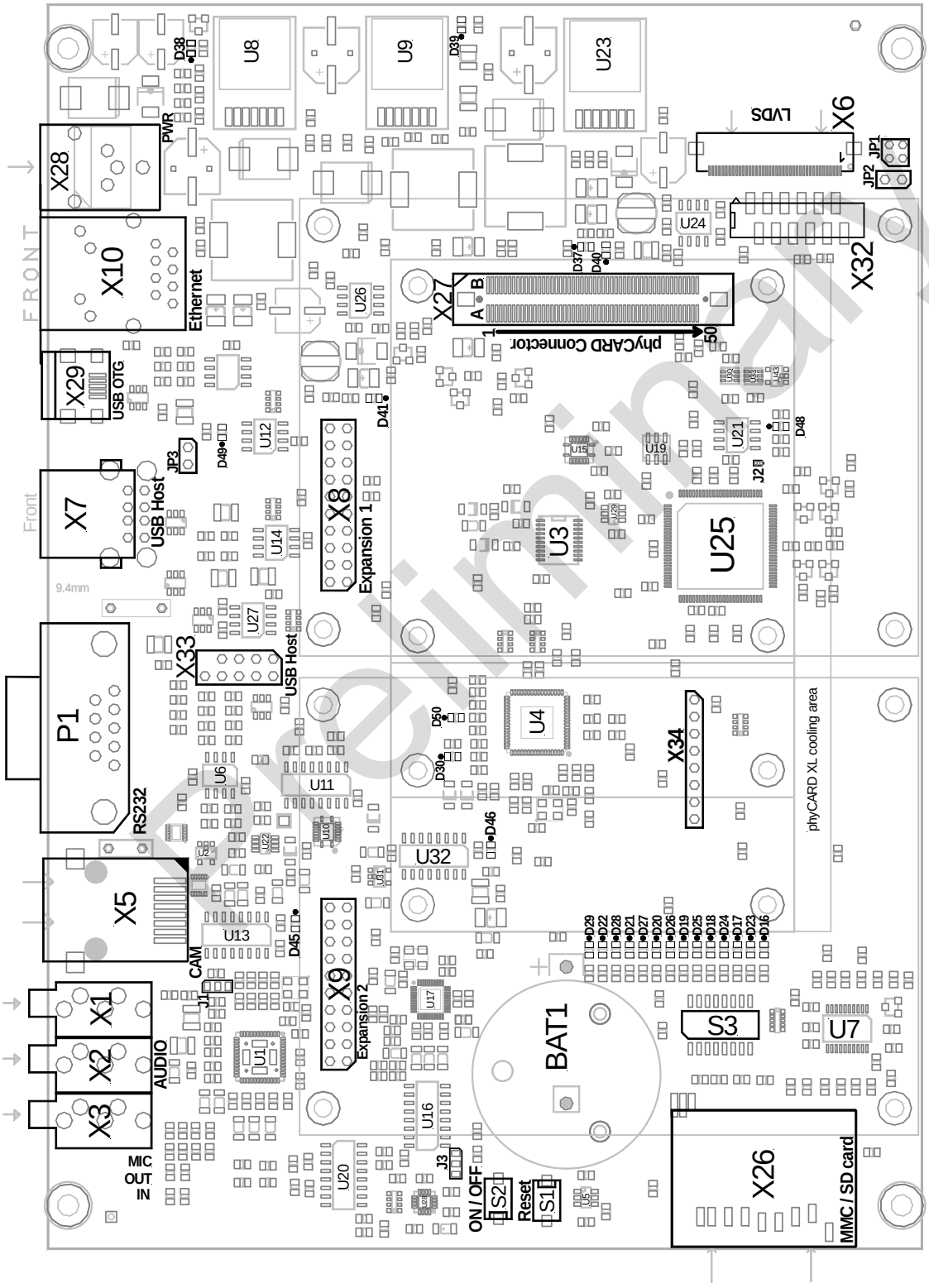

Figure 13: phyBASE Overview of Connectors, LEDs and Buttons

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17.2.1 Connectors and Pin Header

Table 27 lists all available connectors on the phyBASE. *Figure 13* highlights the location of each connector for easy identification.

Reference Designator	Description	See Section
X1	Stereo Microphone input connector	*17.3.8*
X2	Stereo Line out connector	*17.3.8*
X3	Stereo Line In connector	*17.3.8*
X6	Display data connector	*17.3.7.1*
X7	Dual USB Host connector	*17.3.5*
X8A	Extension connector 0	*17.3.12*
X9A	Extension connector 1	*17.3.12*
X10	Ethernet connector, RJ45 with speed and link led	*17.3.4*
X26	Secure Digital/MultiMedia Card slot	*17.3.13*
X27	phyCARD-Connector for mounting the phyCARD-i.MX 6	*17.3.1*
X28	Wall adapter input power jack to supply main board power (+9 - +36 V)	*17.3.2*
X29	USB On-The-Go connector	*17.3.6*
X32	Display / Backlight supply voltage connector	*17.3.7.2*
X33	USB Host connector	*17.3.5*
X34	CPLD JTAG connector	**for internal use only**
P1	Serial Interface, DB-9F	*17.3.3*

Table 27: phyBASE Connectors and Pin Headers

Note:
Ensure that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

Preliminary

17.2.2 Switches

The phyBASE is populated with two switches which are essential for the operation of the phyCARD-i.MX 6 module on the carrier board. *Figure 13* shows the location of the switches and push buttons.

Button	Description	See Section
S1	System Reset Button – system reset signal generation	*17.3.15*
S2	Power Button – powering on and off main supply voltages of the carrier board	*17.3.2*

Table 28: phyBASE Push Buttons Descriptions

S1 Issues a **system reset** signal. Pressing this button will toggle the X_nRESET_IN pin (X2A7) of the phyCARD SOM low, causing the module to reset. Additionally, a peripheral reset is generated by the PLD on the CB to reset peripherals such as the USB Hub, etc.

S2 Issues a **power on/off** event. Pressing this button less than 2 seconds will toggle the nPWR_KEY pin of the phyBASE CPLD LOW, causing the CPLD to turn on the supply voltages. Pressing this button for more than 2 seconds causes the CPLD to turn off the supply voltages.

Additionally a DIP-Switch is available at S3. The following table gives an overview of the functions of the DIP-switch.

Note:
The following table describes only settings suitable for the phyCARD-i.MX 6. Other settings must not be used with the phyCARD-i.MX 6.

Preliminary

Switch	Setting	Description	See Section
S3_1/ S3_2		Depending on the audio standard supported by the phyCARD the audio and touch panel signals are either processed by the Wolfson audio/touch contrl. at U1 (AC'97) or the TI Audio CODEC at U17 (I^2S) and a dedicated touch contrl. at U28. Switches 1 and 2 of DIP-Switch S3 select which device processes the audio and touch panel signals.	
	0/0	**Auto Detection: based on the low level of the HDA_SEL/AC_INT signal generated on the phyCARD-i.MX 6 the TI audio CODEC (U17) is selected to process the I^2S compliant audio signals, while the dedicated touch contrl. at U28 handles the signals from a touch screen.**	*17.3.7.3* *17.3.8*
	1/0	Regardless of the signal HDA_SEL/AC_INT the TI audio CODEC (U17) is selected to process the I^2S compliant audio signals, while the dedicated touch contrl. at U28 handles the signals from a touch screen.	
S3_3/ S3_4		Switches 3 and 4 of DIP-Switch S3 configure the I^2C address for the communication between CPLD and phyCARD.	
	0/0	**CPLD Address 0x40 (7 MSB)**	
S3_5		Switch 5 of DIP-Switch S3 selects the interface used for the communication between CPLD and phyCARD.	
	0	**I^2C communication selected**	
S3_6		Switch 6 of DIP-Switch S3 turns the SPI Multiplexer on, or off.	
	0	**SPI multiplexer off**	
S3_7/ S3_8		Switches 7 and 8 of DIP-Switch S3 map the two slave select signals of the SPI interface and the two GPIO_IRQ signals (GIO0_IRQ, GPIO1_IRQ) to two of the three available connectors.	
	0/0	**SS0/GPIO0 -> extension 0 (X8A),** **SS1/GPIO1 -> extension 1 (X9A)**	*17.3.7.1* *17.3.10* *17.3.11* *17.3.12*
	0/1	SS0/GPIO0 -> extension 0 (X8A), SS1/GPIO1 -> display data connector (X6)	
	1/x	SS0/GPIO0 -> extension 1 (X9A), SS1/GPIO1 -> display data connector (X6)	

Table 29: phyBASE DIP-Switch S3 Descriptions[1]

[1]: Default settings are in **bold blue** text

Preliminary

17.2.3 LEDs

The phyBASE is populated with numerous LEDs to indicate the status of the various USB-Host interfaces, as well as the different supply voltages. *Figure 13* shows the location of the LEDs. Their function is listed in the table below:

LED	Color	Description	See Section
D16	yellow	USB1 amber led	
D17	yellow	USB2 amber led	
D18	yellow	USB3 amber led	
D19	yellow	USB4 amber led	
D20	yellow	USB5 amber led	
D21	yellow	USB6 amber led	
D22	yellow	USB7 amber led	
D23	green	USB1 green led	
D24	green	USB2 green led	*17.3.5*
D25	green	USB3 green led	
D26	green	USB4 green led	
D27	green	USB5 green led	
D28	green	USB6 green led	
D29	green	USB7 green led	
D30	red	Active/Suspend status LED of the USB hub at U4	
D50	red	Hi-Speed indicator LED for USB hub's upstream port connection speed	
D49	red	Indicates presence of VBUS at the USB OTG interface	*17.3.6*
D37	green	5 V supply voltage for peripherals on the phyBASE	
D38	green	supply voltage of the phyCARD	
D39	green	3.3 V supply voltage for peripherals on the phyBASE	*17.3.2*
D40	green	3.3 V standby voltage of the phyBASE	
D41	green	standby voltage of the phyCARD	
D45	yellow	SSI interface compliant with the AC'97 standard	*17.3.8*
D46	green	SSI interface compliant with the I^2S standard	
D48	yellow	user LED driven by the LED dimmer at U21	

Table 30: phyBASE LEDs Descriptions

Preliminary

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17.2.4 Jumpers

The phyCARD Carrier Board comes pre-configured with 2 removable jumpers (JP) and 3 solder jumpers (J). The jumpers allow the user flexibility of configuring a limited number of features for development constraint purposes. *Table 31* ists the jumpers, their default positions, and their functions in each position. *Figure 14* depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board.

Figure 15 provides a detailed view of the phyBase jumpers and their default settings. In these diagrams a beveled edge indicates the location of pin 1.

Before making connections to peripheral connectors it is advisable to consult the applicable section in this manual for setting the associated jumpers.

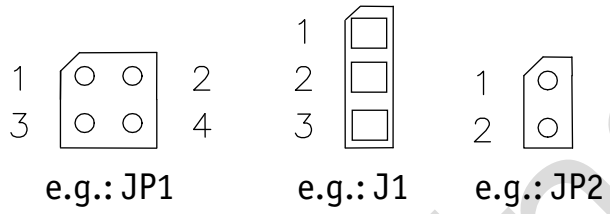

Figure 14: Typical Jumper Numbering Scheme

Table 31 provides a comprehensive list of all carrier board jumpers. The table only provides a concise summary of jumper descriptions. Only jumpers supporting features of the phyCARD-i.MX 6 are described. For a detailed description of each jumper see the applicable chapter listing in the right hand column of the table.

If manual modification of the solder jumpers is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the board inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Preliminary

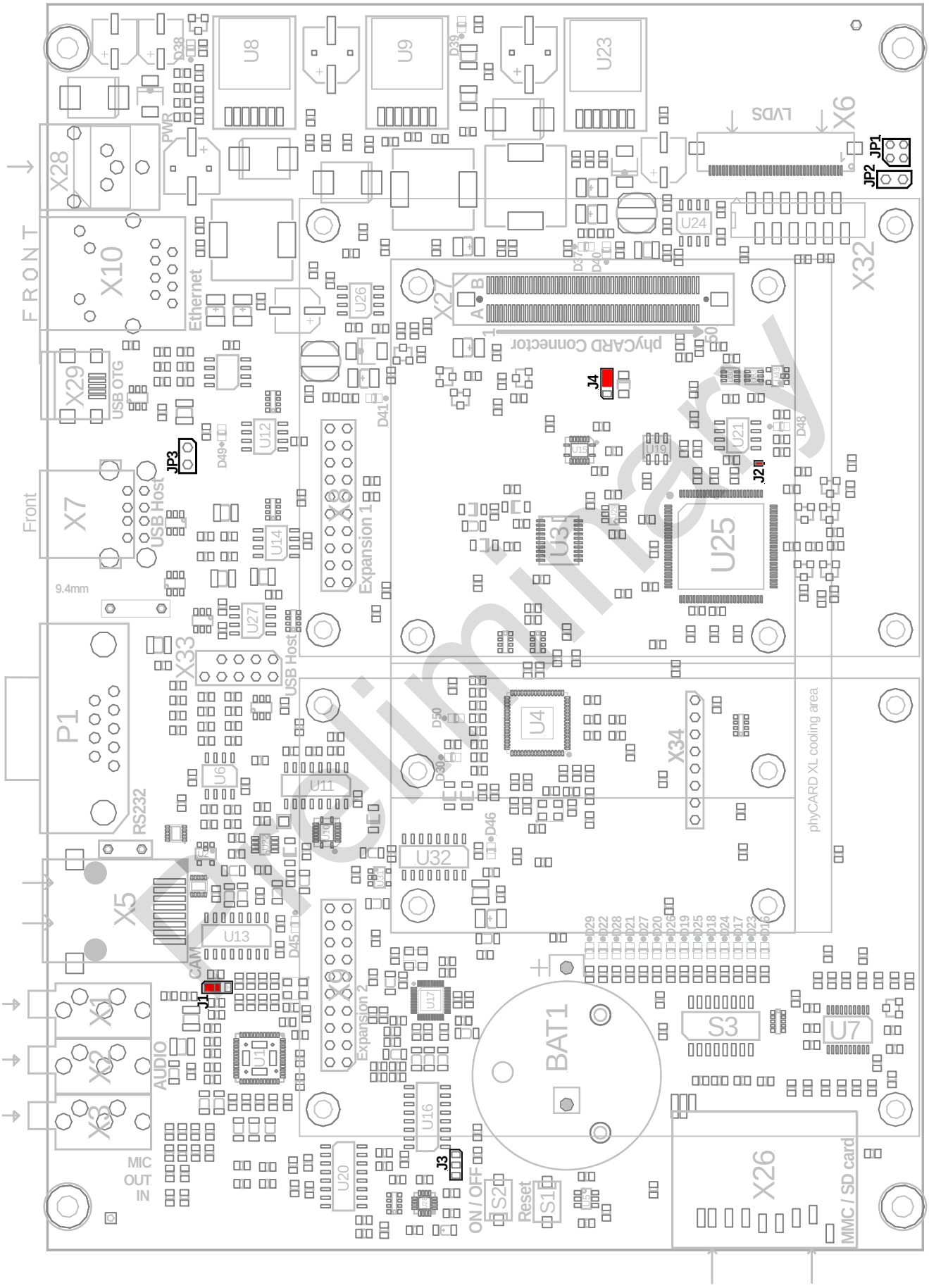

Figure 15: phyBASE Jumper Locations

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The following conventions were used in the Jumper column of the jumper table (*Table 31*)
- J = solder jumper
- JP = removable jumper

Jumper	Setting	Description	See Section
JP1	**open**	Jumper JP1 selects the boot device of the phyCARD-i.MX 6 **NAND** [1]	*17.3.14*
	1+2	SD0 external [1]	
	3+4	Serial USB OTG (USB0) [1]	
	1+2, 3+4	Bootconfig from eFUSE	
		other settings must not be used with the phyCARD-i.MX 6	
JP2	**open**	Jumper JP2 connects the input voltage to connector X32 as supply voltage for a backlight. **VCC12V Backlight disabled**	*17.3.7.2*
	closed	VCC12V Backlight connected to power supply. **Only 12V DC power supplies allowed**	
JP3	**open**	Jumper JP3 forces the USB OTG interface of the phyCARD-i.MX 6 to function either as host (master), or device (slave). **USB_OTG_ID floating, phyCARD-i.MX 6 in slave mode, or according to the mode configured by software**	*17.3.6*
	closed	USB_OTG_ID connected to GND, phyCARD-i.MX 6 in host mode	
J2	**closed**	Jumper J2 configures the I^2C address of the LED dimmer at U21 **I^2C device address of LED dimmer set to 0x60**	*17.3.7.2* *17.3.9*
	open	I^2C device address of LED dimmer set to 0x61	
J3	**1+2**	Jumper J3 configures the I^2C address of the touch screen controller at U28 **I^2C device address set to 0x44**	*17.3.7.3* *17.3.9*
	2+3	I^2C device address set to 0x41	

Table 31: phyBASE Jumper Descriptions[1]

[1]: please see *section 6* for more information on the different boot modes

Preliminary

Jumper	Setting	Description	See Section
J4	1+2	Jumper J4 selects the reset source of the audio devices at U1 and U17. The source of the reset can be either the peripheral reset signal X_nRES_OUT (X27B7), or the dedicated audio device reset SSI_RESET[2] (X27B44) from the phyCARD-i.MX 6. Dedicated audio device reset SSI_RESET (X27B44) from the phyCARD-i.MX 6 connected to the reset input of the audio devices at U1 and U17	*17.3.7.3*
	2+3	**Peripheral reset signal X_nRES_OUT (X27B7) from the phyCARD-i.MX 6 connected to the reset input of the audio devices at U1 and U17**	

Table 31: phyBASE Jumper Descriptions[3] (continued)

Note:
Detailed descriptions of the assembled connectors, jumpers and switches can be found in the following chapters.

Preliminary

[1]: Default settings are in **bold blue** text
[2]: The reset signal at X27B44 originates from GPIO3_21 of the i.MX 6
[3]: Default settings are in **bold blue** text

17.3 Functional Components on the phyBASE Board

This section describes the functional components of the phyCARD Carrier Board supporting the phyCARD-i.MX 6. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

17.3.1 phyCARD-i.MX 6 SOM Connectivity (X27)

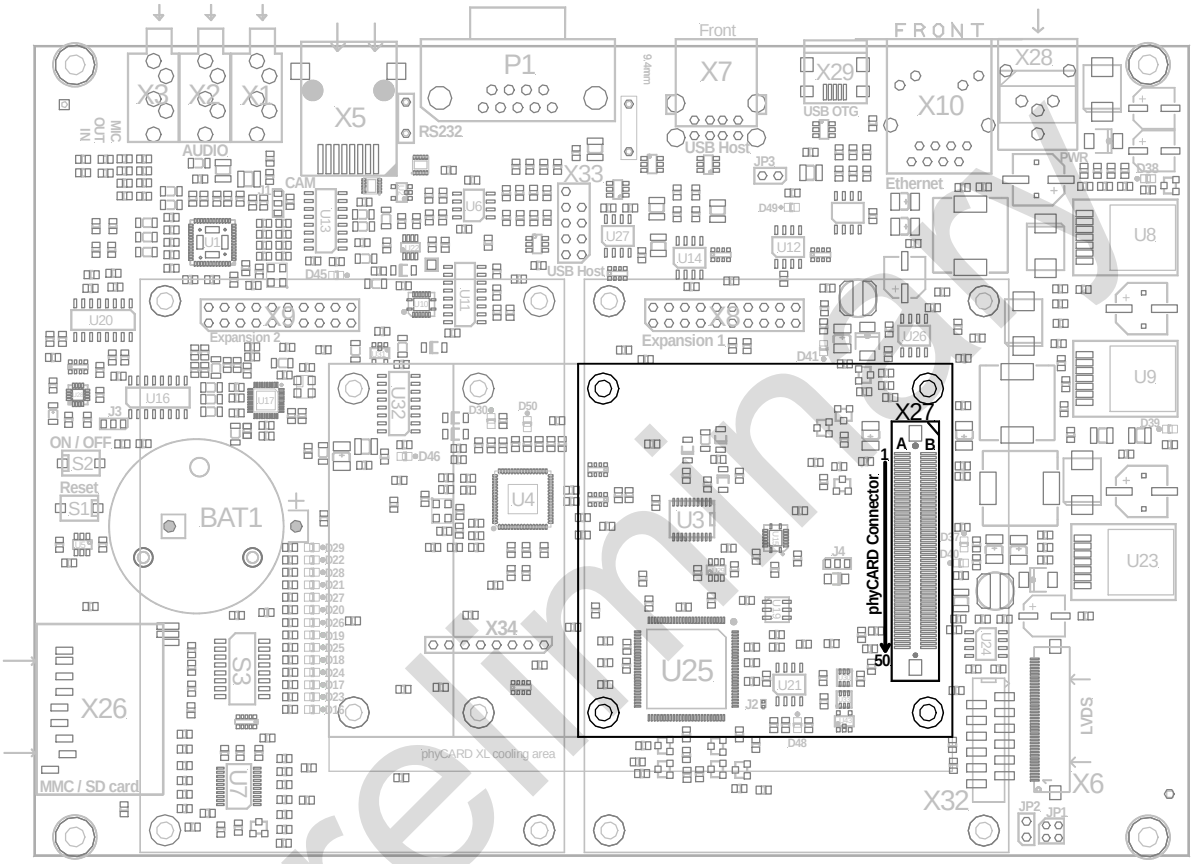


Figure 16: phyCARD-i.MX 6 SOM Connectivity to the Carrier Board

Connector X27 on the carrier board provides the phyCARD System on Module connectivity. The connector is keyed for proper insertion of the SOM. *Figure 16* above shows the location of connector X27, along with the pin numbering scheme as described in *section 2*.

Preliminary

17.3.2 Power Supply (X28)

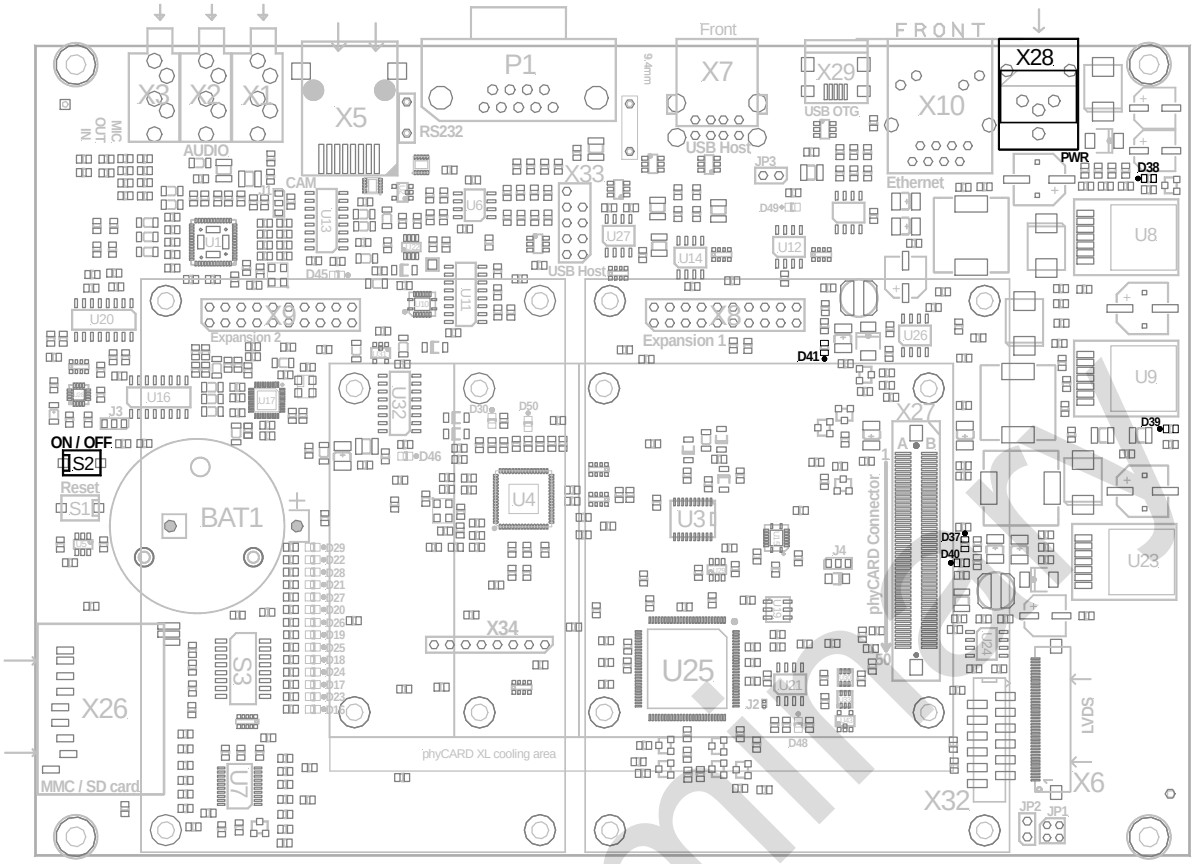


Figure 17: Powering Scheme

Caution:
Do not use a laboratory adapter to supply power to the carrier board! Power spikes during power-on could destroy the phyCARD module mounted on the carrier board! Do not change modules or jumper settings while the carrier board is supplied with power!

Permissible input voltage at X28: +9 V - +36 V DC unregulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCARD mounted on the carrier board as well as whether an optional extension board is connected to the carrier board. An adapter with a minimum supply of 2.0 A is recommended.

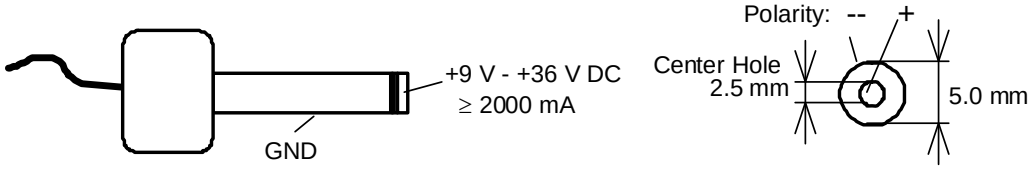


Figure 18: Power Connector corresponding to Wall Adapter Input X28

No jumper configuration is required in order to supply power to the phyCARD module!

Preliminary

The phyBASE is assembled with a few power LEDs whose functions are described in the following table:

LEDs	Color	Description	
D37	green	VCC5V -	5V supply voltage for peripherals on the phyBASE
D38	green	VCC_PHYCARD -	supply voltage of the phyCARD
D39	green	VCC3V3 -	3V3 supply voltage for peripherals on the phyBASE
D40	green	VCC3V3STBY -	3V3 standby voltage of the phyBASE
D41	green	VSTBY -	standby voltage of the phyCARD

Table 32: LEDs Assembled on the Carrier Board

Note:
For powering up the phyCARD the following actions have to be done:

1. Plug in the power supply connector
   » All power LEDs should light up and the phyCARD puts serial output to serial line 0 at P1.
2. For powering down the phyCARD-i.MX 6 button S2 should be pressed for a minimum time of 2000 ms.
3. Press button S2 for a maximum time of 1000 ms.
   » All power LEDs should light up and the phyCARD puts serial output to serial line 0 at P1.

Three different power states are possible **RUN**, **OFF** and **SUSPEND**.

- During **RUN** all supply voltages except VSTBY are on. This means that the phyCARD-i.MX 6 is supplied by VCC_PHYCARD.
- In **OFF** state all supply voltages are turned off. Only the standby voltage (VCC3V3STBY) of the phyBASE itself is still available to supply the PLD, the RTC and to provide a high-level voltage for the Reset and Power switch.
- In **SUSPEND** mode only the standby voltage VSTBY for the phyCARD-i.MX 6 and the standby voltage (VCC3V3STBY) of the phyBASE itself are generated. This means the phyCARD-i.MX 6 is supplied only by VSTBY.

The RUN and OFF state can be entered using the power button S2 as described in the gray box above. It is also possible to enter OFF state with the help of the phyCARD's X_nPOWER_OFF signal (GPIO1_25 of the i.MX 6). To enter OFF state signal X_nPOWER_OFF must be active (low) for at least 100 ms.

SUSPEND state can be entered using signal X_nSUSPEND_RAM at pin X27B26 of the phyCARD Connector (GPIO1_24 of the i.MX 6). X_nSUSPEND_RAM must be active (low) for at least 100 ms.

Preliminary

17.3.3 RS-232 Connectivity (P1)

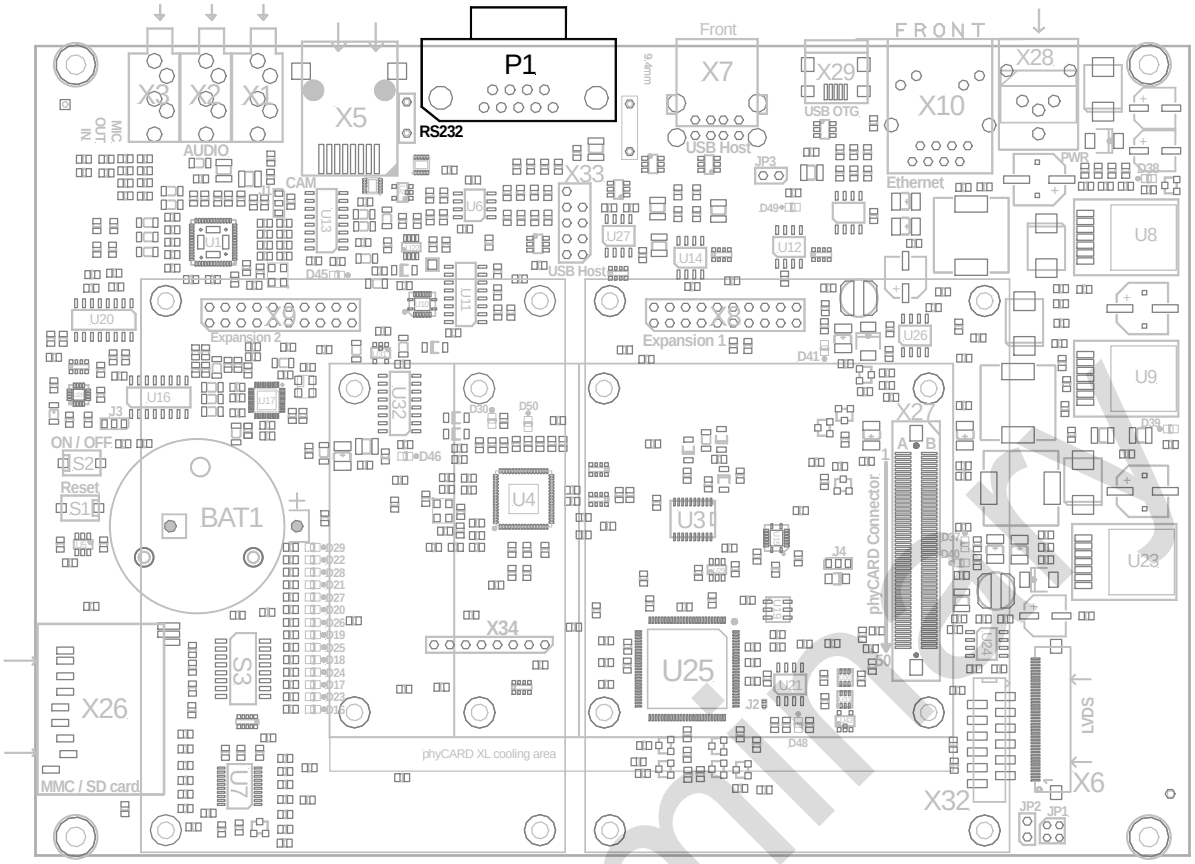
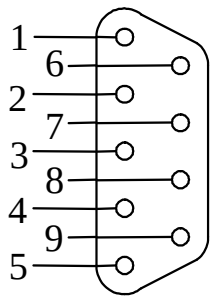


Figure 19: RS-232 Interface Connector P1

Connector P1 is a DB9 sub-connector and provides a connection interface to UART3 of the i.MX 6. The TTL level signals from the phyCARD-i.MX 6 are converted to RS-232 level signals. As defined in the specification of the X-Arc bus the serial interface allows for a 5-wire connection including the signals RTS and CTS for hardware flow control. *Figure 20* below shows the signal mapping of the RS-232 level signals at connector P1.

The RS-232 interface is hard-wired and no jumpers must be configured for proper operation.



Pin 2:	TxD-RS232
Pin 7:	RTS-RS232
Pin 3:	RxD-RS232
Pin 8:	CTS-RS232
Pin 5:	GND

Figure 20: RS-232 Connector P1 Signal Mapping

Preliminary

17.3.4 Ethernet Connectivity (X10)

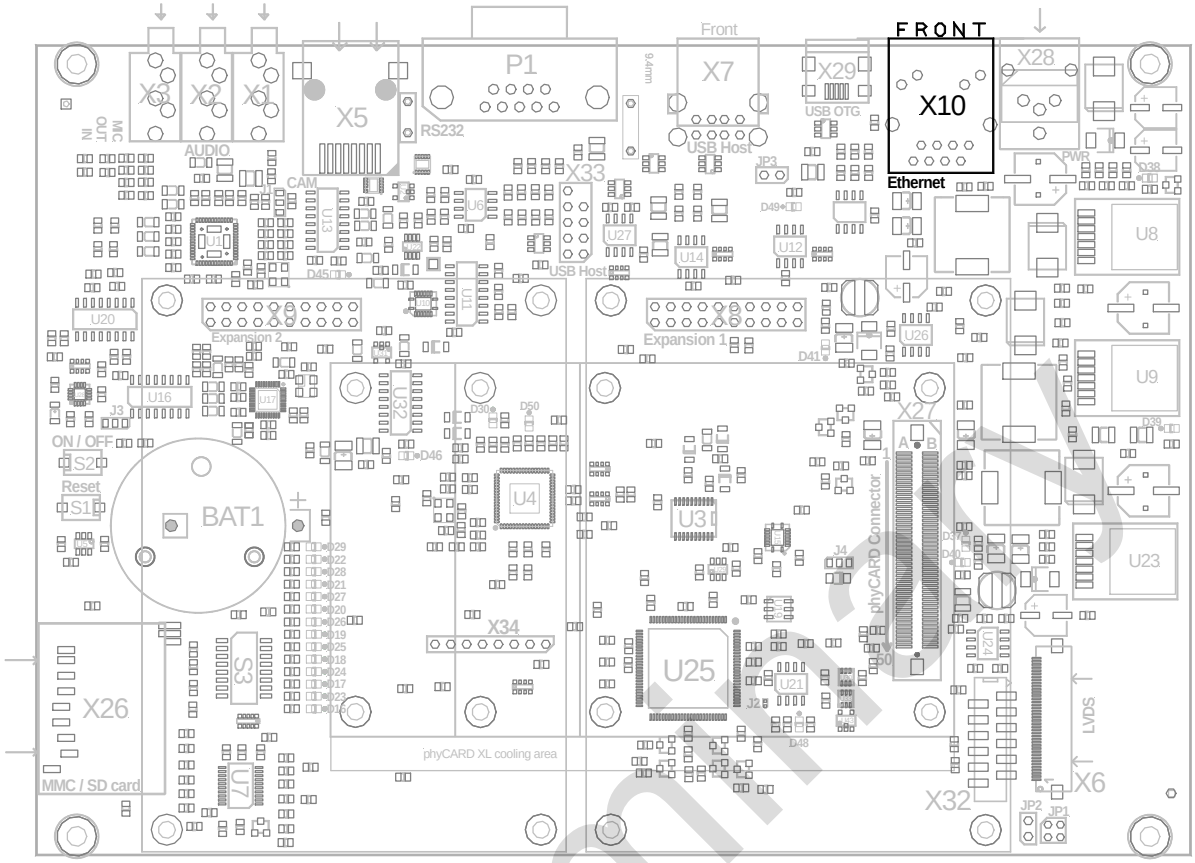


Figure 21: Ethernet Interface at Connector X10

The Ethernet interface of the phyCARD is accessible at an RJ45 connector (X10) on the carrier board. Due to its characteristics this interface is hard-wired and can not be configured via jumpers. The LEDs for LINK (green) and SPEED (yellow) indication are integrated in the connector.

Preliminary

17.3.5 USB Host Connectivity (X6, X7, X8, X9, X33)

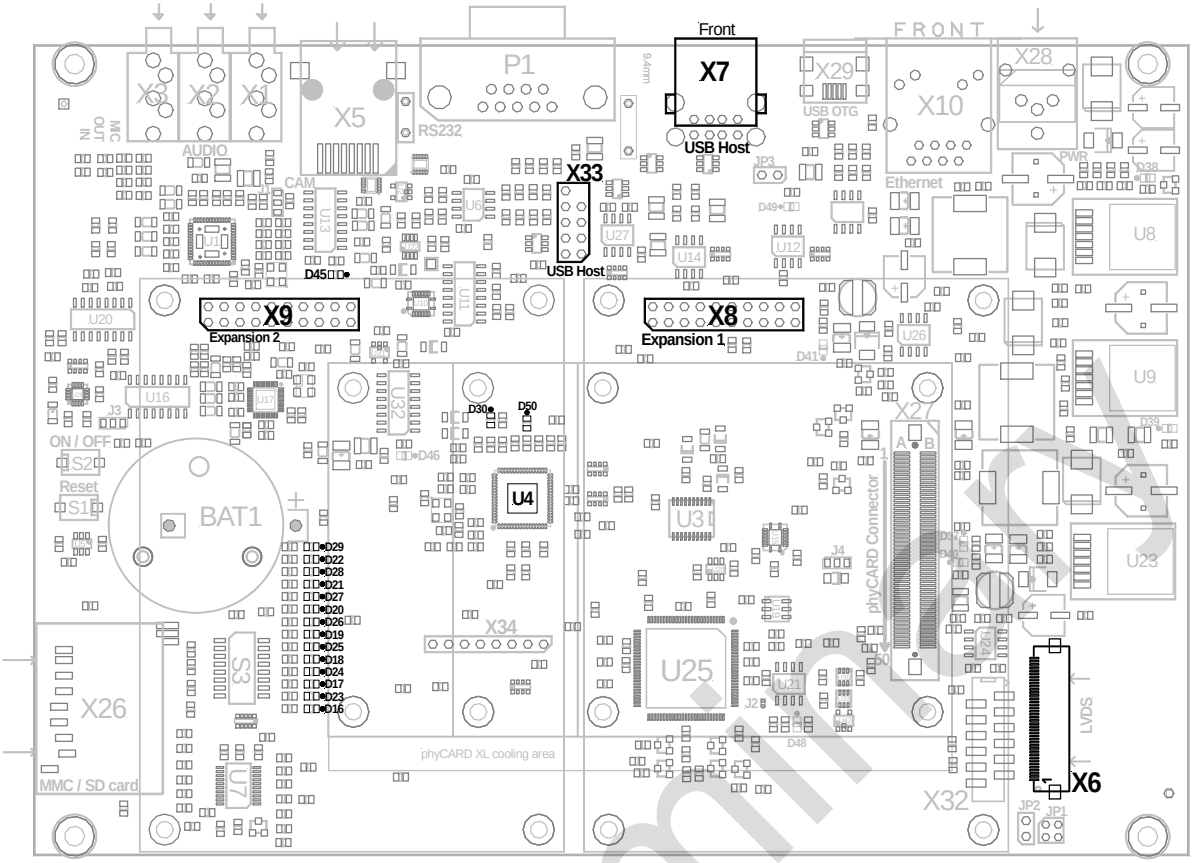


Figure 22: Components supporting the USB Host Interface

The USB host interface of the phyCARD is accessible via the USB hub controller U4 on the carrier board. The controller supports control of input USB devices such as keyboard, mouse or USB key. The USB hub has 7 downstream facing ports. Two ports extend to standard USB connectors at X7 (dual USB A). Two more ports connect to 9 pin header row X33. These interfaces are compliant with USB revision 2.0. The remaining ports are accessible at the display data connector X6 and the extension connectors X8A and X9A. These three interfaces provide only the data lines D+ and D-. They do not feature a supply line Vbus.

Preliminary

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LEDs D16 to D29 as well as D30 and D50 signal use of the USB host interfaces. *Table 30* shows the assignment of the LEDs to the different USB ports.

Table 33 shows the distribution of the seven downstream facing ports to the different connectors, whereas *Table 34* shows the pinout of USB host connector X33.

USB hub port #	Connector	Connector Type	LEDs
USB1 / USB 5	X33	9 pin header row (see table below)	D16, D23 D20, D27
USB2	X6	40 pin FCC (pins 16 (D+) and 17 (D-))	D17, D24
USB3	X8	20 pin header row (pins 19 (D-) and 20 (D+))	D18, D25
USB4	X9	20 pin header row (pins 19 (D-) and 20 (D+))	D19, D26
USB6	X7A (bottom)	USB A	D21, D28
USB7	X7B (top)	USB A	D22, D29

Table 33: Distribution of the USB Hub's (U4) Ports

Pin #	Signal name	Description
1	USB5_VBUS	USB5 Power Supply
3	USB5_D-	USB5 Data -
5	USB5_D+	USB5 Data +
2	USB1_VBUS	USB1 Power Supply
4	USB1_D-	USB1 Data -
6	USB1_D+	USB1 Data +
7, 8	GND	Ground
9,10	NC	Not connected

Table 34: Universal USB Pin Header X33 Signal Description

Preliminary

17.3.6 USB OTG Connectivity (X29)

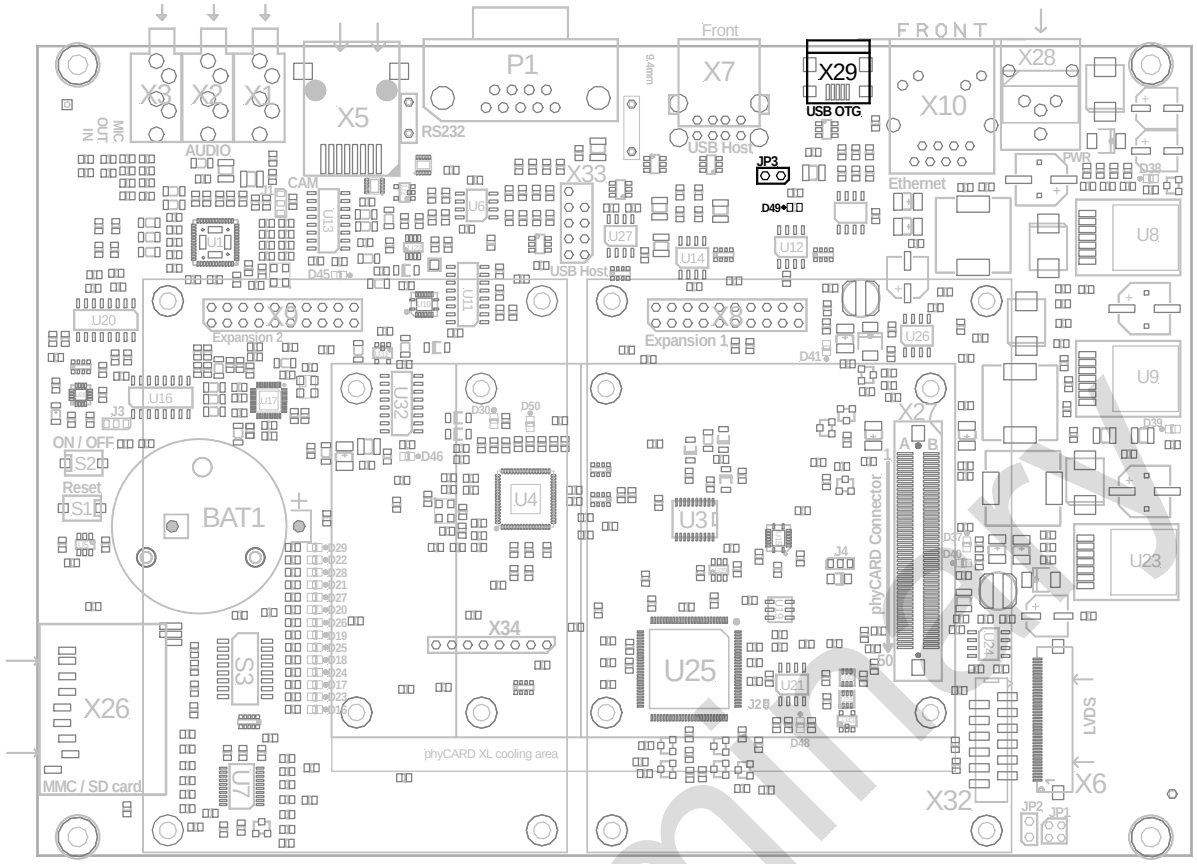

Figure 23: USB OTG Interface at Connector X29

The USB OTG interface of the phyCARD is accessible at connector X29 (USB Mini AB) on the carrier board. The phyCARD-i.MX 6 supports the On-The-Go feature. The Universal Serial Bus On-The-Go is a device capable to initiate the session, control the connection and exchange Host/Peripheral roles between each other. This interface is compliant with USB revision 2.0.

Jumper JP3 configures the OTG operating mode. By default this jumper is open, which leaves the USB_OTG_ID pin floating, and thus configuring the OTG interface as slave. Alternatively this jumper can be closed, connecting the signal X_UID to GND, and configuring the OTG interface as host. Typically the configuration of a connecting device as host or slave is done automatically via a USB OTG cable. However, given the limited number of OTG enabled devices in the embedded market this jumper is provided to either simulate an OTG cable, or force the OTG interface into host mode when OTG operation is not required.

LED D49 signals VBUS power supply, which is generated via a power distribution switch TPS2042 (U29) of the carrier board. The power distribution switch is controlled via the signals X_USB_HS_nPSW and X_USB_HS_FAULT which extend directly from the phyCARD connector.

Preliminary

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17.3.7 Display / Touch Connectivity (X6, X32)

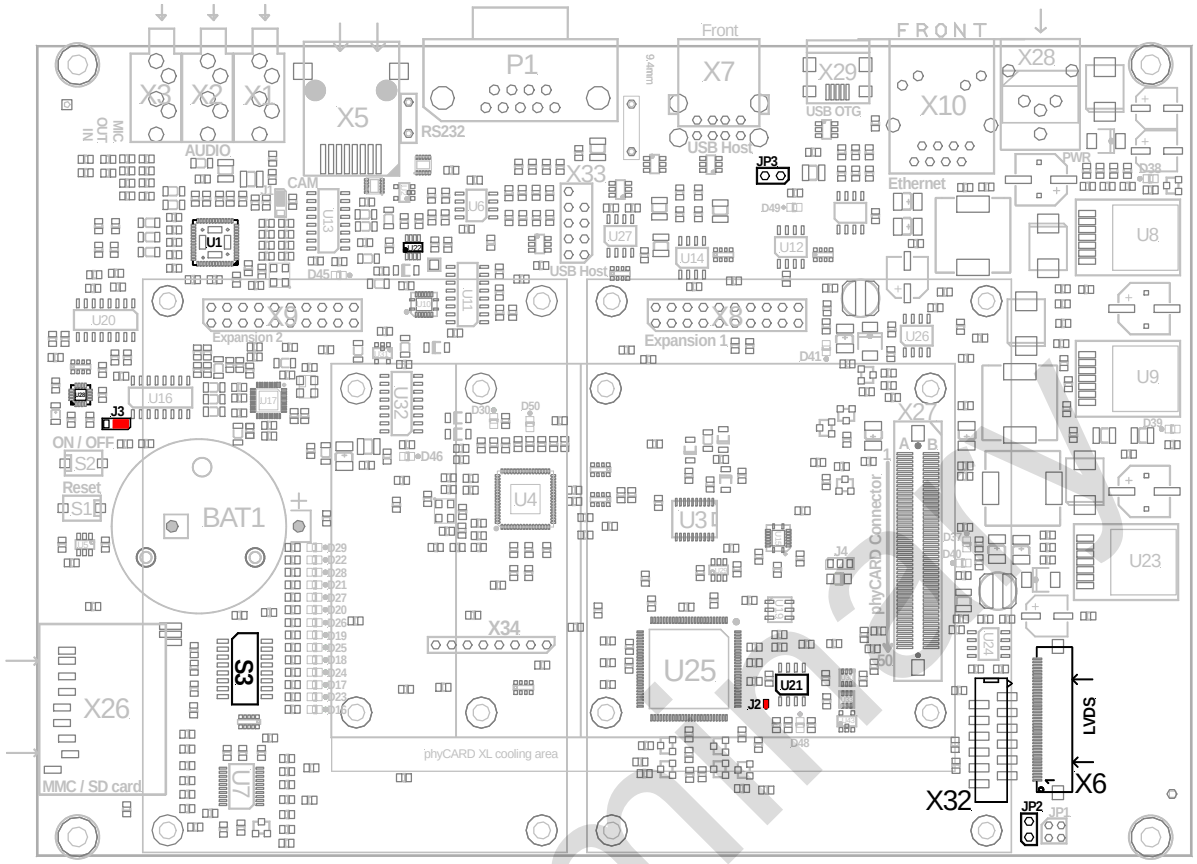

Figure 24: Universal LVDS Interface at Connector X6

The various performance classes of the phyCARD family allow to attach a large number of different displays varying in resolution, signal level, type of the backlight, pinout, etc. In order not to limit the range of displays connectable to the phyCARD, the phyBASE has no special display connector suitable only for a small number of displays. The new concept intends the use of an adapter board (e.g. PHYTEC's LCD display adapters LCD-014 and LCD-017) to attach a special display, or display family to the phyCARD. A new PHYTEC Display-Interface (PDI) was defined to connect the adapter board to the phyBASE. It consists of two universal connectors which provide the connectivity for the display adapter. They allow easy adaption also to any customer display. One connector (40 pin FCC connector 0.5 mm pitch) at X6 is intend for connecting all data signals to the display adapter. It combines various interface signals like LVDS, USB, I^2C, etc. required to hook up a display. The second connector of the PDI (AMP microMatch 8-338069-2) at X32 provides all supply voltages needed to supply the display and a backlight, and the brightness control.

The following sections contain specific information on each connector.

Preliminary

17.3.7.1 PDI Data Connector (X6)

PDI data connector X6 provides display data which originates from the parallel display interface of the i.MX 6 (LIDD). The display signals are converted into LVDS on the phyCARD-i.MX 6 and are available at the X-Arc bus (phyCARD-Connector). Hence, no additional signal conversion is necessary on the phyBASE. The LVDS signals extend directly from the phyCARD-Connector to the PDI Data Connector (X6).

Along with the display and touch screen interface signals other useful interfaces such as USB, I²C, etc. are available at PDI data connector X6. *Table 36* lists all miscellaneous signals and gives detailed explanations. The following table shows the pin-out of the PDI's display data connectors at X6.

Pin #	Signal name	I/O	SL	Description
1	SPI1_SCLK	O	3.3 V	SPI 1 clock
2	SPI_MISO	I/O	3.3 V	SPI 1 master data in; slave data out
3	SPI1_MOSI	O/I	3.3 V	SPI 1 master data out; slave data in
4	SP1I_SS_DISP	O	3.3 V	SPI 1 chip select display
5	DISP_IRQ	I	3.3 V	Display interrupt input
6	VCC3V3	O	3.3 V	Power supply display
7	I2C_SCL	I/O	3.3 V	I²C clock signal
8	I2C_SDA	I/O	3.3 V	I²C data signal
9	GND	-	-	Ground
10	LS_BRIGHT[1]	O	3.3 V	PWM brightness output
11	VCC3V3	O	3.3 V	Logic supply voltage[2]
12	nPWR_KEY	I	3.3 V	Power on/off button
13	nDISP_ENA	O	3.3 V	Display enable signal
14	PHYWIRE	I/O	3.3 V	Hardware Introspection Interface **for internal use only**
15	GND	-	-	Ground
16	USB2_D+	I/O	3.3 V	USB2 data +[3]
17	USB2_D-	I/O	3.3 V	USB2 data -[2]
18	GND	-	-	Ground
19	TXOUT0-	O	3.3 V	LVDS data channel 0 negative output
20	TXOUT0+	O	3.3 V	LVDS data channel 0 positive output
21	GND	-	-	Ground
22	TXOUT1-	O	3.3 V	LVDS data channel 1 negative output

Table 35: Display Data Connector X6 Signal Description

[1]: This signal is also available at the display power connector X32 (refer to section *17.3.7.2* for more information)
[2]: Provided to supply any logic on the display adapter. Max. draw 100 mA
[3]: LEDs D17 and D24 signal use of the USB interface

Preliminary

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23	TXOUT1+	O	3.3 V	LVDS data channel 1 positive output
24	GND	-	-	Ground
25	TXOUT2-	O	3.3 V	LVDS data channel 2 negative output
26	TXOUT2+	O	3.3 V	LVDS data channel 2 positive output
27	GND	-	-	Ground
28	TXOUT3-	O	3.3 V	LVDS data channel 3 negative output
29	TXOUT3+	O	3.3 V	LVDS data channel 3 positive output
30	GND	-	-	Ground
31	TXCLKOUT-	O	3.3 V	LVDS clock channel negative output
32	TXCLKOUT+	O	3.3 V	LVDS clock channel positive output
33	GND	-	-	Ground
34	TP_X+	I/O	3.3 V	Touch
35	TP_X-	I/O	3.3 V	Touch
36	TP_Y+	I/O	3.3 V	Touch
37	TP_Y-	I/O	3.3 V	Touch
38	TP_WP	I/O	3.3 V	Touch
39	GND	-	-	Ground
40	LS_ANA	I	3.3 V	Light sensor analog input

Table 35: Display Data Connector X6 Signal Description (continued)

The table below shows the auxiliary interfaces at display data connector X6.

Signal	Description
USB2_D	USB host interface derived from downstream port 2 of the USB hub at U4. Suitable for optional features e.g. front USB (refer to section *17.3.5* for more information about the USB host interfaces)
I2C	I^2C interface for an optional EEPROM, or other I^2C devices (additional information on the I^2C interfaces can be found in section *17.3.9*)
SPI1	SPI interface to connect optional SPI slave
PHYWIRE	Hardware Introspection Interface **for internal use only**
nPWR_KEY	Power on/off signal to allow for an ON/OFF switch on a front panel. It connects to the nPWR_KEY input of the PLD at U25 (parallel to the ON/OFF switch S2)
nDISP_ENA	Can be used to enable, or disable the display, or to shutdown the backlight. nDISP_ENA is connected to the corresponding input of the PLD at U25 x
LS_BRIGHT	PWM output to control the brightness of a display's backlight (0% = dark, 100% = bright). The signal is derived from the first output LED0 of the LCD dimmer at U21[1].
LS_ANA	Analog light sensor input. The analog light sensor input at pin 40 extends to an 8-bit A/D converter which is connected to the I^2C bus at address 0x64. To get the maximum adjustment range the output voltage of an applicable light sensor should range from 0 V to VRef (VCC_3V3AD).

Table 36: Auxiliary Interfaces at PDI Data Connector X12

[1]: This signal is also available at the display power connector X32 (refer to section *17.3.7.2* for more information)

Preliminary

The connection of the SPI interface and the display interrupt input to the X-Arc bus is shared with the SPI interfaces and the interrupt inputs on the extension connectors X8A and X9A. Because of that these signals have to be mapped to the display data connector by configuring switches 7 and 8 of DIP-Switch S3. *Table 37* shows the required settings.

The default setting does not connect the SPI interface and the GPIO/Interrupt pin of the X-Arc bus to the display data connector.

Button	Setting	Description
S3_7/ S3_8	**0/0**	**SS0/GPIO0_IRQ[1] -> extension 0 (X8A), SS1/GPIO1_IRQ[1] -> extension 1 (X9A)**
	0/1	SS0/GPIO0_IRQ[1] -> extension 0 (X8A), SS1/GPIO1_IRQ[1] -> display data connector (X6)
	1/x	SS0/GPIO0_IRQ[1] -> extension 1 (X9A), SS1/GPIO1_IRQ[1] -> display data connector (X6)

Table 37: SPI and GPIO Connector Selection

17.3.7.2 Display Power Connector (X32)

The display power connector X32 (AMP microMatch 8-188275-2) provides all supply voltages needed to supply the display and a backlight, as well as one PWM signal for brightness control.

Pin #	Signal name	I/O	SL	Description
1	GND	-		Ground
2	VCC3V3	O	3.3 V	3.3 V power supply display
3	GND	-		Ground
4	VCC5V	O	5 V	5V power supply display
5	GND	-		Ground
6	VCC5V	O	5 V	5 V power supply display
7	GND	-		Ground
8	VCC5V	O	5 V	5 V power supply display
9	GND	-		Ground
10	LS_BRIGHT	O	3.3 V	PWM brightness output
11	VCC12V_BL	O	+9 V - +38 V	Backlight power supply
12	VCC12V_BL	O	+9 V - +38 V	Backlight power supply

Table 38: LVDS Power Connector X32 Signal Description

To make VCC12V_BL available at X32 jumper JP2 must be closed.

[1]: GPIO0_IRQ0 ≙ GPIO2_24 (at J23) and GPIO1_IRQ1 ≙ GPIO1_6 (at T3) of the i.MX 6

Preliminary

Caution!
The backlight voltage VCC12V_BL corresponds to the input voltage at power jack X28. There is no protective circuitry for the backlight. Close jumper JP2 only if a 12 V power supply is connected to X28 as primary supply for the phyBASE.

The PWM signal at pin 10 can be used to control the brightness of a display's backlight. It is generated by an LED dimmer (U21). The LED dimmer is connected to the I²C bus at address[1] 0x60 (7 MSB).

17.3.7.3 Touch Screen Connectivity

As many smaller applications need a touch screen as user interface, provisions are made to connect 4- or 5- wire resistive touch screens to the display data connector X6 (pins 34 - 38, refer to *Table 35*). Two touch screen controllers are available on the phyCARD Carrier Board. The audio/touch codec at U1 allows connecting 4- and 5-wire touch panels, whereas a separate touch panel controller at U28 is suitable for 4-wire touch panels only. Because of the dual functionality of the audio / touch controller the choice which controller is used to handle the signals from the touch screen is pegged to the audio standard supported by the phyCARD. For phyCARDs supporting the AC'97 standard the audio/touch controller at U1 processes the touch panel signals. For phyCARDs delivering I²S compliant audio signals the dedicated touch panel controller at U28 must be selected.

Switches 1 and 2 of DIP-Switch S3 select which controller is used to process the touch panel signals. The different configurations are shown in *Table 39*.

Button	Setting	Description
S3_1/ S3_2		Depending on the audio standard supported by the phyCARD the audio and touch panel signals are either processed by the Wolfson audio/touch contrl. at U1 (AC'97), or the TI Audio CODEC at U17 (I²S) and a dedicated touch contrl. at U28. Switches 1 and 2 of DIP-Switch S3 select which device processes the audio and touch panel signals.
	0/0	**Auto Detection: based on the low level of the HDA_SEL/AC_INT signal generated on the phyCARD-i.MX 6 the dedicated touch contrl. at U28 handles the signals from a touch screen.**
	1/0	The dedicated touch contrl. at U28 handles the signals from a touch screen, regardless of the signal HDA_SEL/AC_INT.

Table 39: Selection of the Touch Screen Controller

As the phyCARD-i.MX 6 features an I²S compliant audio interface the dedicated touch controller at U28 (STMPE811) must be chosen to process the touch screen signals. It is connected to the X-Arc bus's I²C interface. The I²C address can be configured with jumper J3. The default setting is 0x44 (7 MSB)[1].

The touch controller provides an interrupt output which extends directly to the interrupt input pin GPIO2_IRQ (X1A47) at the phyCARD Connector.

[1]: Please refer to *Table 31* for information on alternativ I²C address configurations.

Preliminary

17.3.8 Audio Interface (X1, X2, X3)

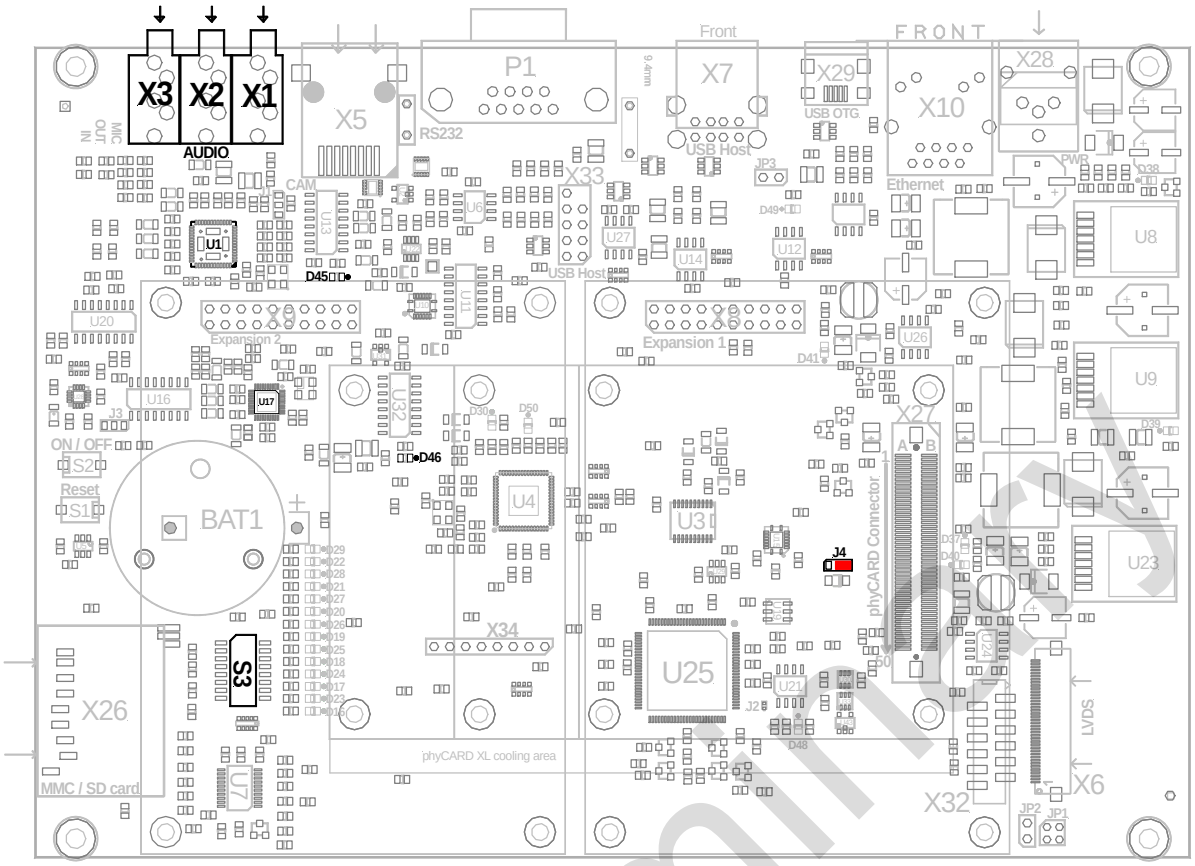

Figure 25: Audio Interface at Connectors X1, X2, X3

The audio interface provides a method of exploring the i.MX 6's I^2S capabilities.

Depending on the audio standard supported by the phyCARD the audio interface on the X-Arc bus connects either to a Wolfson WM9712L audio / touch controller (U1) or a TI TLV320AIC3007 (U17) Audio CODEC on the carrier board. The audio / touch controller at U1 processes AC'97 compliant signals, while signals according to the I^2S standard are handled by the Audio CODEC at U17.

Switches 1 and 2 of DIP-Switch S3 select which codec is used to process the audio signals. *Table 40* shows the different options.

Preliminary

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Button	Setting	Description
S3_1/ S3_2		Depending on the audio standard supported by the phyCARD the audio and touch panel signals are either processed by the Wolfson audio/touch contrl. at U1 (AC'97) or the TI Audio CODEC at U17 (I^2S) and a dedicated touch contrl. at U28. Switches 1 and 2 of DIP-Switch S3 select which device processes the audio and touch panel signals.
	0/0	**Auto Detection: based on the low level of the HDA_SEL/AC_INT signal generated on the phyCARD-i.MX 6 the TI audio CODEC (U17) is selected to process the I^2S compliant audio signals.**
	1/0	The TI audio CODEC (U17) is selected to process the I^2S compliant audio signals, regardless of the signal HDA_SEL/AC_INT.

Table 40: Selection of the Audio Codec

As the phyCARD-i.MX 6 features an I^2S compliant audio interface the Audio CODEC at U17 must be chosen to process the audio signals.

LEDs D45 (AC'97) and D46 (I^2S) indicate which audio interface is active. For the phyCARD-i.MX 6 LED D46 should be on.

To reset the audio ICs at U1 and U17 two different reset sources can be selected with jumper J4. The source of the reset can be either the peripheral reset signal X_nRES_OUT (X27B7), or the dedicated audio device reset SSI_RESET (X27B44) from the phyCARD-i.MX 6. The default setting of jumper J4 selects the peripheral reset signal X_nRES_OUT (X27B7) from the phyCARD-i.MX 6 [1].

Audio devices can be connected to 3.5 mm audio jacks at X1, X2, and X3.

Audio outputs:
X2 – Line output - Line_OUTL/Line_OUTR

Audio Inputs:
X1 - Microphone Inputs - MIC1/MIC2
X3 - Line Input - Line_INL/Line_INR

Please refer to the audio codec's reference manual for additional information regarding the special interface specification.

Preliminary

[1]: Please refer to *Table* for information on alternative settings.

17.3.9 I²C Connectivity

The I²C interface[1] of the X-Arc bus is available at different connectors on the phyBASE. The following table provides a list of the connectors and pins with I²C connectivity.

Connector	Location
Camera interface X5	pin 4 (I²C_SDA); pin 5 (I²C_SCL)
Display data connector X6	pin 8 (I²C_SDA); pin 7 (I²C_SCL)
Extension connector 1 X8A	pin 7 (I²C_SDA); pin 8 (I²C_SCL)
Extension connector 2 X9A	pin 7 (I²C_SDA); pin 8 (I²C_SCL)

Table 41: I²C Connectivity

To avoid any conflicts when connecting external I²C devices to the phyBASE the addresses of the on-board I²C devices must be considered. Some of the addresses can be configured by jumper. *Table 42* lists the addresses already in use. The table shows only the default address. Please refer to *section 17.2.4* for alternative address settings.

Device	Address used (7 MSB)	Jumper
LED dimmer (U21)	0x60	J2
RTC (U3)	0x51	
A/D converter (U22)	0x64	
Touch screen controller (U28)	0x44	J3
CPLD (U25)	0x40	S3_3, S3_4

Table 42: I²C Addresses in Use

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[1]: The interface of the i.MX 6's third I²C module (I2C3) is used for I²C connectivity on the carrier board (refer also to *section 9.5*).

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17.3.10 SPI Connectivity

The SPI interface of the X-Arc bus is available at the extension connectors X8A and X9A as well as at the display data connector X6 (refer to *sections 17.3.7.1* and *17.3.12* to see the pinout). Due to the X-Arc bus specification only two slave select signals are available. Because of that the CPLD maps the SPI interface to two of the connectors depending on the configuration of switches 7 and 8 of DIP-Switch S3. The table below shows the possible configurations.

Button	Setting	Description
S3_7/ S3_8	**0/0**	**SS0/GPIO0_IRQ[1] -> extension 0 (X8A), SS1/GPIO1_IRQ[1] -> extension 1 (X9A)**
	0/1	SS0/GPIO0_IRQ[1] -> extension 0 (X8A), SS1/GPIO1_IRQ[1] -> display data connector (X6)
	1/x	SS0/GPIO0_IRQ[1] -> extension 1 (X9A), SS1/GPIO1_IRQ[1] -> display data connector (X6)

Table 43: SPI Connector Selection

17.3.11 User programmable GPIOs

Two (GPIO0_IRQ and GPIO1_IRQ) of the three GPIO / Interrupt signals available at the X-Arc bus are freely available. They are mapped to the extension connectors X8A and X9A (pin 16), or to the display data connector X6 (pin 5) depending in the configuration at DIP-Switch S3 (see *Table 43*). The third GPIO / Interrupt signal (GPIO2_IRQ[2]) is used to connect the interrupt output of the touch screen controller at U28 to the phyCARD-i.MX 6.

Preliminary

[1]: GPIO0_IRQ0 ≙ GPIO2_24 (at J23) and GPIO1_IRQ1 ≙ GPIO1_6 (at T3) of the i.MX 6 (refer to *section 10*))

[2]: GPIO2_IRQ ≙ GPIO4_29(at R22) of the i.MX 6 (refer to *section 10*))

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17.3.12 Extension connectors (X8A, X9A)

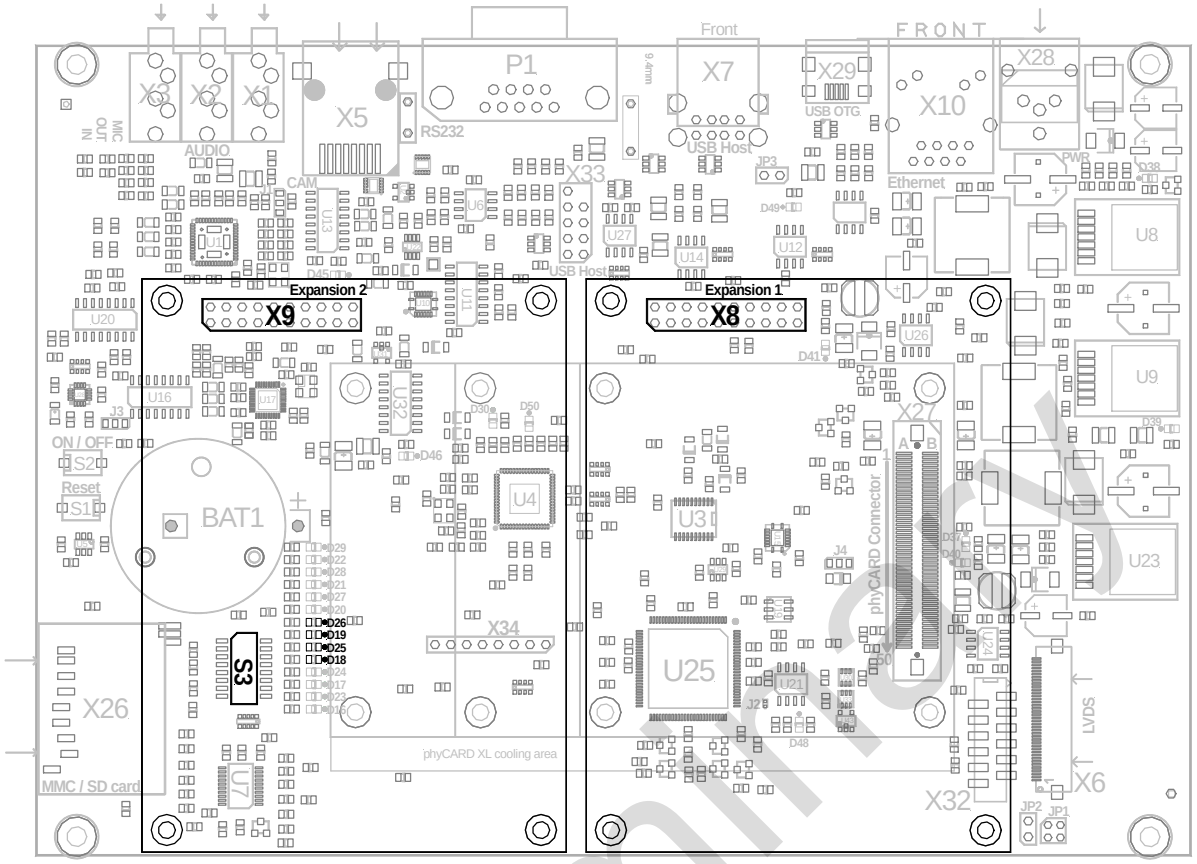

Figure 26: Extension Connector X8A, X9A

The extension connectors X8A and X9A provide an easy way to add other functions and features to the phyBASE[1]. Standard interfaces such as USB, SPI and I^2C as well as different supply voltages and one GPIO are available at the pin header rows. The pinout of the extension connectors is shown in *Table 45*.

As can be seen in *Figure 26* the location of the connectors allows to expand the functionality without expanding the physical dimensions. Mounting wholes can be used to screw the additional PCBs to the phyBASE.

The extension connectors share the SPI interface and the GPIOs of the X-Arc bus with the display data connector X6. Therefore switches 7 and 8 of DIP-Switch S3 must be configured to map the signals to the desired connector.

The following table shows the possible configurations.

[1]: PHYTEC offers a variety of extension boards (PEBs) to add new features, such as CAN, additional GPIOs or Ethernet, etc. Please visit our web side or contact our sales team.

Preliminary

Button	Setting	Description
S3_7/ S3_8	**0/0**	**SS0/GPIO0_IRQ[1] -> extension 0 (X8A), SS1/GPIO1_IRQ[1] -> extension 1 (X9A)**
	0/1	SS0/GPIO0_IRQ[1] -> extension 0 (X8A), SS1/GPIO1_IRQ[1] -> display data connector (X6)
	1/x	SS0/GPIO0_IRQ[1] -> extension 1 (X9A), SS1/GPIO1_IRQ[1] -> display data connector (X6)

Table 44: SPI and GPIO Connector Selection

Pin #	Signal Name	Description
1	VCC5V	5 V power supply
2	VCC5V	5 V power supply
3	VCC3V3	3.3 V power supply
4	VCC3V3	3.3 V power supply
5	GND	Ground
6	GND	Ground
7	I2C_SDA	I²C Data
8	I2C_SCL	I²C Clock
9	PHYWIRE	Hardware Introspection Interface. **For internal use only**
10	GND	Ground
11	SPI_SS_SLOT0 SPI_SS_SLOT1	X8A: SPI chip select extension port 0 X9A: SPI chip select extension port 1
12	SPI1_MOSI	SPI master output/slave input
13	SPI1_SCLK	SPI clock output
14	SPI1_MISO	SPI master input/slave output
15	/SPI1_RDY	SPI data ready input master mode only
16	SLOT0_IRQ SLOT1_IRQ	X8A: Interrupt input extension port 0 X9A: Interrupt input extension port 1
17	GND	Ground
18	GND	Ground
19	USB3_D- USB4_D-	X8A: USB3 Data D-[2] X9A: USB4 Data D-[3]
20	USB3_D+ USB4_D+	X8A: USB3 Data D+[1] X9A: USB4 Data D+[2]

Table 45: PHYTEC Extension Connectors X8A, X9A

[1]: GPIO0_IRQ0 ≙ GPIO2_24 (at J23) and GPIO1_IRQ1 ≙ GPIO1_6 (at T3) of the i.MX 6 (refer to *section 10*))
[2]: LEDs D18 and D25 signal use of the USB3 interface (X8A)
[3]: LEDs D19 and D26 signal use of the USB4 interface (X9A)

Preliminary

17.3.13 Secure Digital Memory Card/ MultiMedia Card (X26)

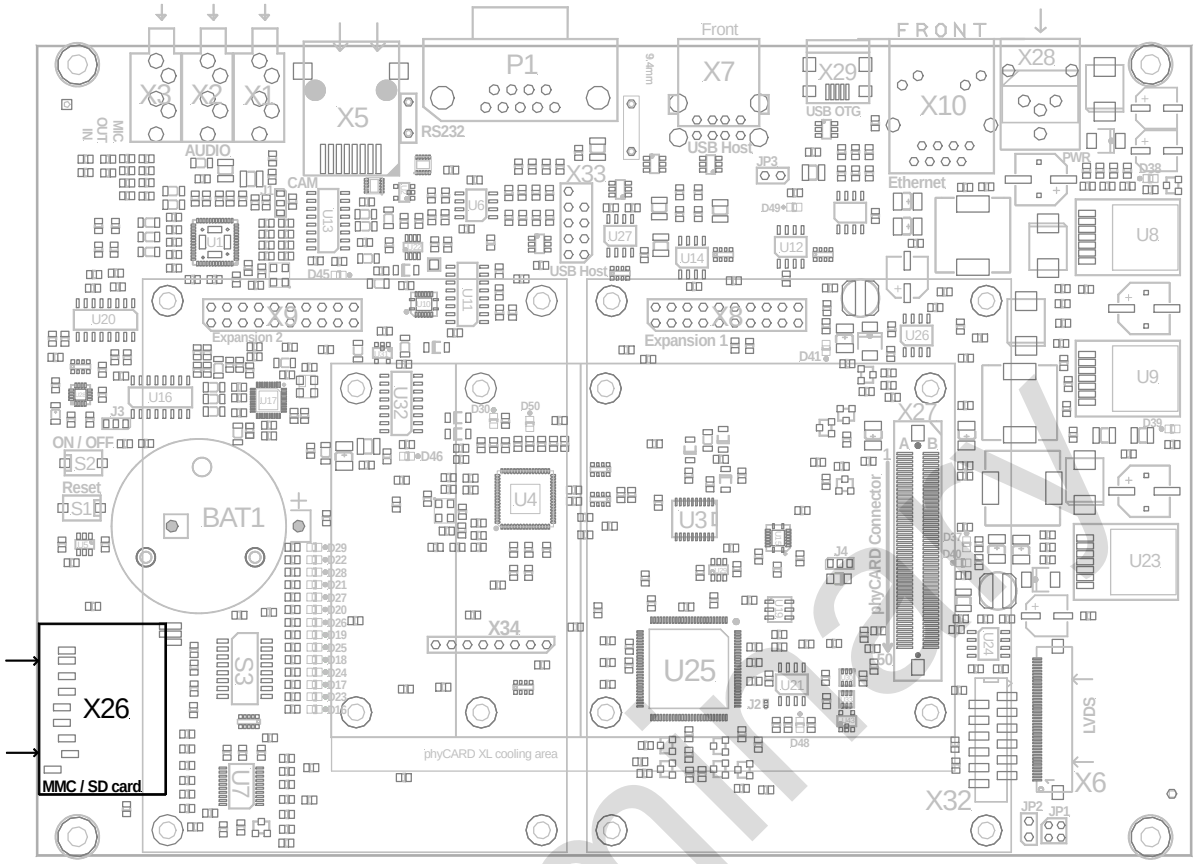

Figure 27: SD / MM Card interface at connector X26

The phyCARD Carrier Board provides a standard SDHC card slot at X26 for connection to SD/MMC interface cards. It allows easy and convenient connection to peripheral devices like SD- and MMC cards in 1-bit, or 4-bit bus mode. Power to the SD interface is supplied by sticking the appropriate card into the SD/MMC slot. The card slot X26 connects to the phyCARD-i.MX 6 via a level shifter to ensure the correct voltage for the SD/MMC cards.

Preliminary

17.3.14 Boot Mode Selection (JP1)

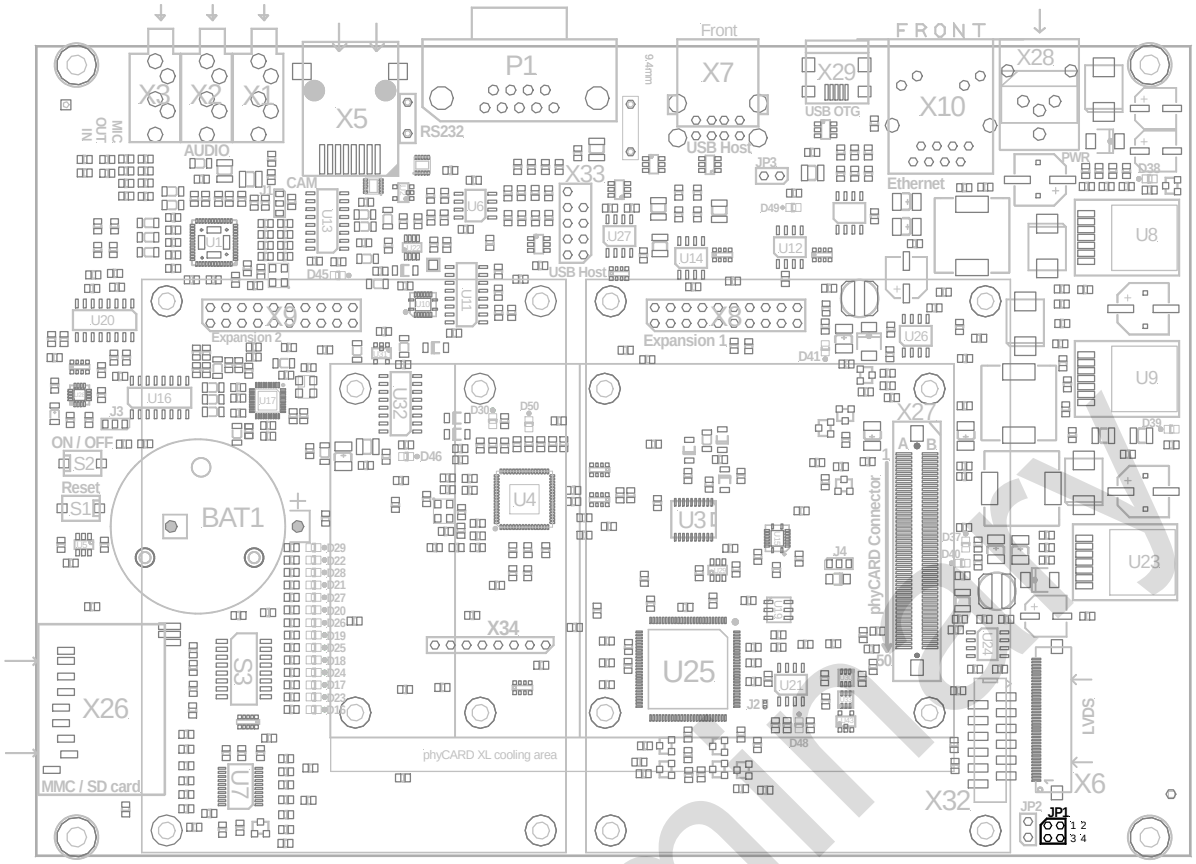

Figure 28: Boot Mode Selection Jumper JP1

The boot mode jumper JP1 is provided to configure the boot mode of the phyCARD-i.MX 6 after a reset.

By default the boot mode jumper is open, configuring the phyCARD-i.MX 6 for booting from the NAND device. *Table 46* shows the different boot options for the phyCARD-i.MX 6. Please refer to *section 6* as well as the i.MX 6 Reference Manual for more information about possible configurations.

Preliminary

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Jumper	Setting	Description
JP1	**open**	Jumper JP1 selects the boot device of the phyCARD-i.MX 6 **NAND** [1]
	1+2	SD0 external [1]
	3+4	Serial USB OTG (USB0) [1]
	1+2, 3+4	Bootconfig from eFUSE [1]
		other settings must not be used with the phyCARD-i.MX 6

Table 46: Boot Options for the phyCARD-i.MX 6

Preliminary

[1]: please see *section 6* for more information on the different boot modes

17.3.15 System Reset Button (S1)

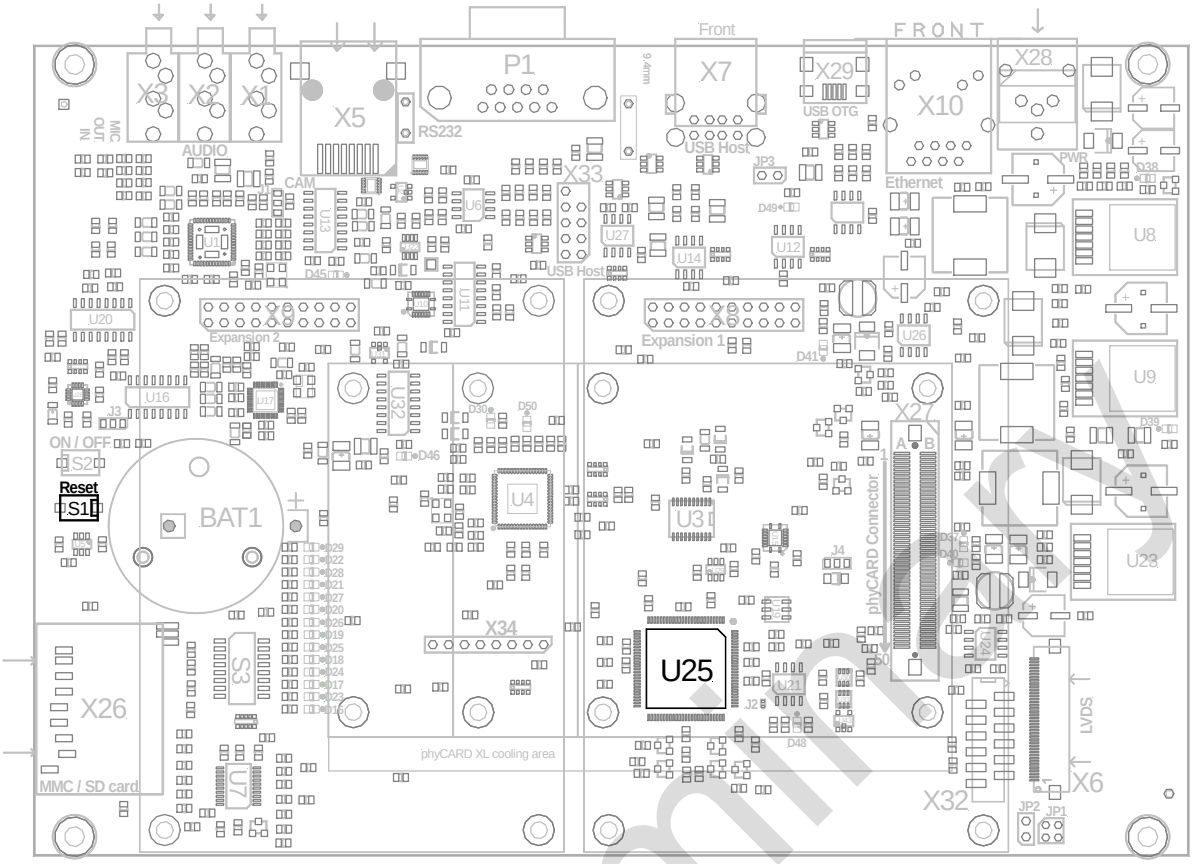

Figure 29: System Reset Button S1

The phyCARD Carrier Board is equipped with a system reset button at S1. Pressing this button will toggle the X_nRESET_IN pin (X1A7) of the phyCARD SOM low, causing the module to reset. Additionally, a peripheral reset is generated by the PLD (U25) on the CB to reset peripherals such as the USB Hub, etc.

Preliminary

17.3.16 RTC at U3

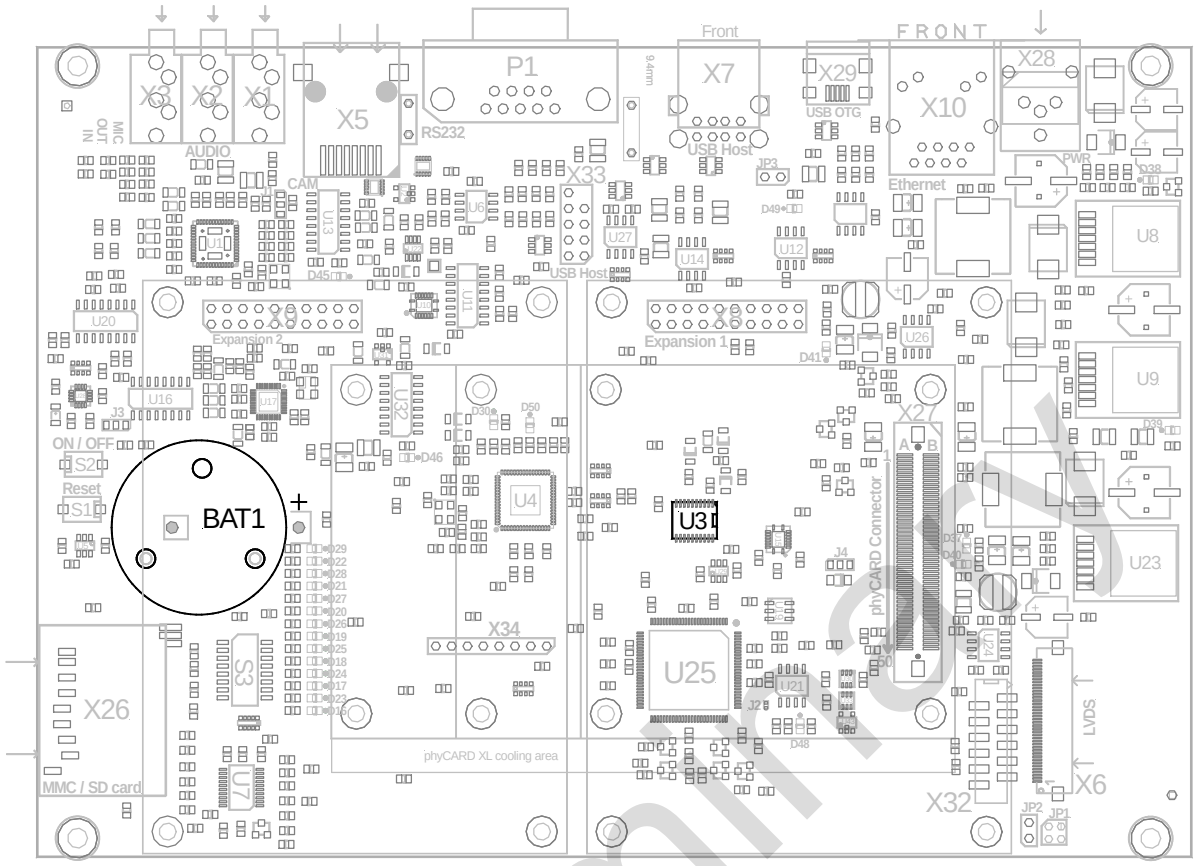

Figure 30: RTC with Battery Buffer

For real-time or time-driven applications, the phyBASE is equipped with an RTC-8564 Real-Time Clock at U3. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0x51 (7 MSB)
- Power consumption
  Bus active (400 kHz): < 1 mA
  Bus inactive, CLKOUT inactive: = 275 nA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

The Real-Time Clock is programmed via the I^2C bus (address 0x51). Since the phyCARD-i.MX 6 is equipped with an internal I^2C controller, the I^2C protocol is processed very effectively without extensive processor action (refer also to *section 9.5*)

Preliminary

The Real-Time Clock also provides an interrupt output that extends to the Wakeup input of the PLD at U25 and is used within the PLD's state machine. Additionally the interrupt is inverted and brought out as low active signal X_nWakeUp at pin X27A48[1] on the phyCARD Connctor An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications.

The RTC_CLK signal, which is also connected to the PLD at U25, can be programmed to various frequencies e.g. 1 Hz.

Caution!
As the RTC_CLK signal is used for the timing of the PLD's internal processes great care must be taken to ensure that the timing doesn't get corrupted by changing the frequency.

Note:
After connection of the supply voltage the Real-Time Clock generates no interrupt. The RTC must be first initialized (*see RTC Data Sheet for more information*).

Use of a coin cell at BAT1 allows to buffer the RTC.

Preliminary

[1]: extending on the phyCARD-i.MX 6 to the input port PWRON of the PMIC (U29) and port P3.2 of the CMIC (U13)

17.3.17 PLD at U25

The phyBASE is equipped with a Lattice LC4256V PLD at U25. This PLD device provides the following features:

- Power management function (*section 17.3.2*)
- Signal mapping and configuration of the sound devices at U1 (for AC'97) and at U17 (for I^2S) (*section 17.3.8*)
- Signal mapping SPI chip select and interrupt to the extension or display connectors (*sections 17.3.10* and *17.3.11*)
- Touch Signal mapping to the discrete touch controller at U28, or to the touch controller integrated in the audio codec at U1 (*section 17.3.7.3)*

Preliminary

17.3.18 Carrier Board Physical Dimensions

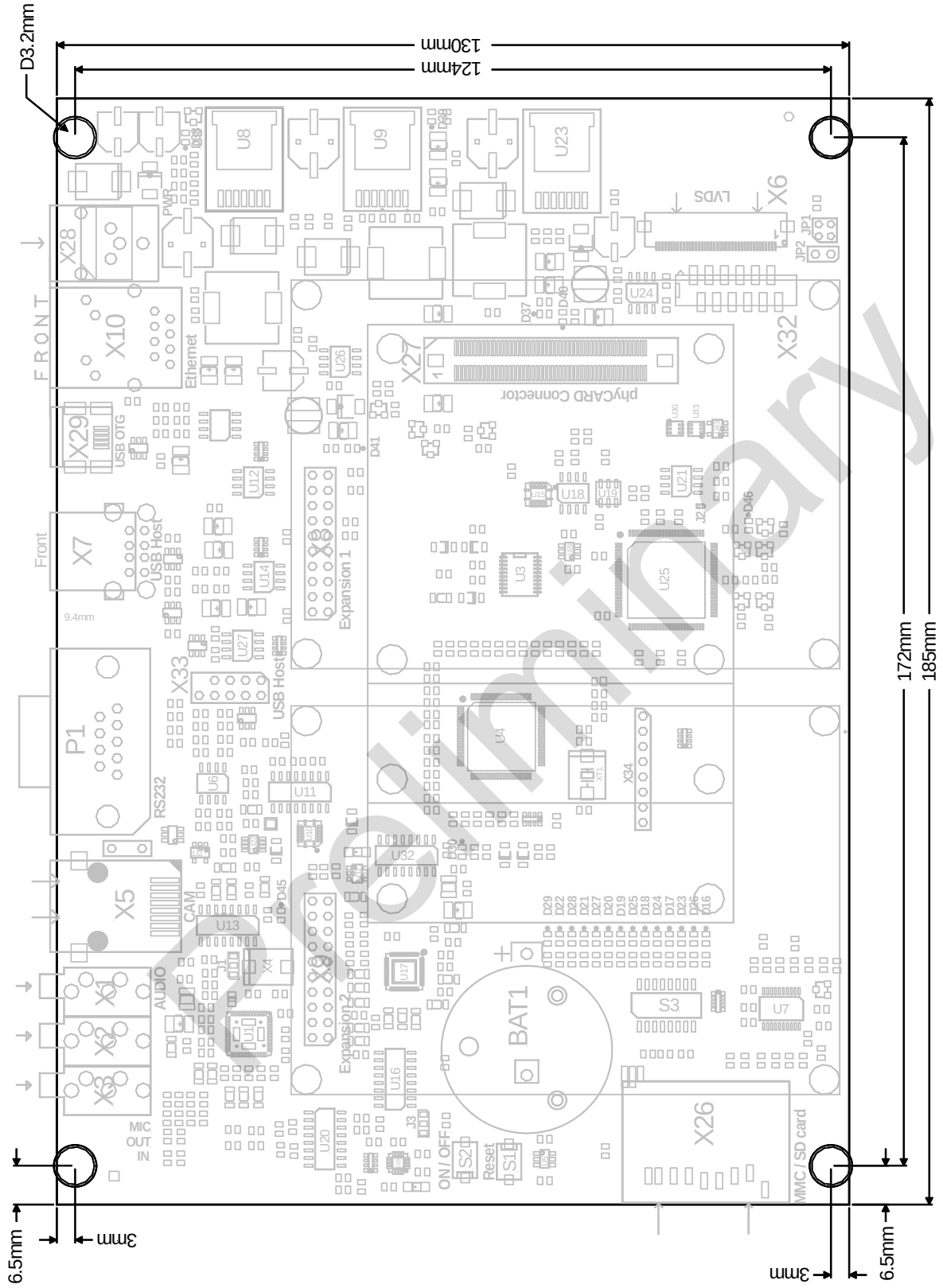

Figure 31: Carrier Board Physical Dimensions

Please contact us if a more detailed dimensioned drawing is needed to integrate the phyBASE into a customer application.

Preliminary

18 Revision History

Date	Version #	Changes in this manual
21.08.2014	Manual L-800e_0	Preliminary edition. Describes the phyCARD-i.MX 6 SOM (PCB 1371.2) with phyBASE- Carrier Board (PCB 1360.2).

Preliminary

Preliminary

Index

1

100Base-T 35
10Base-T 35

9

9 46

A

Audio CODEC 79
Audio Interface 37

B

Backup Voltage 18
Block Diagram 3
Boot Configuration 26
Booting 25

C

Camera Interface 46
Control Management IC 18

D

DDR3 SDRAM 27
DDR3_1V5 19
DDR3_VREF 19
DDR3_VTT 19
Debug Interface 41
Dimensions 48
Display Interface 44

E

EEPROM 27, 28
EEPROM Write Protection 28
EMC xi
Ethernet 35

F

Features 2, 55

G

General Purpose I/Os 39
GND Connection 53

H

Humidity 48

I

I²C EEPROM 28
I²C Interface 36
I²C Memory 16
I²S 37

J

J3 ..... 16, 28
J31 ..... 16, 46
JTAG Interface 41

L

LAN 36
LED
  SOM D1 40
  SOM D2 40
LINK LED 70
LVDS
  Camera Signals 16, 46

M

MAC 36
MAC Address 36

N

NAND Flash 27

O

Operating Temperature 48
Operating Voltage 48

P

PDI 74
phyBASE
  Connectors 58
  P169
  Peripherals 57
  Pin Header 58
  Switches 59
  X10 70
  X27 66
  X28 67
  X29 73
  X32 74
  X33 71

Preliminary

X6 ..... 71, 74
X7 71
X8 71
X9 71
phyCARD-Connector 7, 8
Physical Dimensions 47
PHYTEC Display-Interface 74
Pin Description..... 7
Pinout 10, 11, 12
PLD 92
PMIC 18
Power Consumption..... 48
Power Domains..... 19
Power Management..... 23
Power Management IC 18
Power Supply 6

R

RS-232 Level..... 32
RTC 90

S

SD / MMC Card Interfaces..... 29
SDRAM..... 27
Serial Interfaces 31
SMT Connector 7
SPEED LED 70
SPI Interface..... 37
Storage Temperature 48
Supply Voltage 17
System Configuration 25
System Memory 27
System Power..... 17

T

Technical Specifications 47

U

U10 28
U11 35
U13 27
U17 18
U27 ..... 16, 46
U29 18
U2-U9 27
UART..... 32
USB
OTG Interface 32
USB 2.0 ..... 71, 73
USB Device..... 33
USB Host 32, 33
USB OTG..... 32
User LEDs..... 40

V

VDD_3V3..... 17, 19
Voltage Output..... 21
VSTBY..... 18
VSTBY_IN 19

W

Weight..... 48
WM9712L..... 79

X

X29..... 73
X3 41

Preliminary

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